Design of Hardware Efficient Modulated Filter Bank for EEG Signals Feature Extraction

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Abstract—**In this paper, we propose a new efficient design algorithm to synthesize low complexity FIR filters, which has been applied to EEG signals feature extraction filter bank. A prudently defined bit-level frequency response sensitivity function is designed as a measure for the proposed coefficients quantization decision making. The coefficients are synthesized to meet the specifications while addressing the complexity reduction by maximizing common subexpressions sharing with the aid of instant checking and updating of common subepxressions statistics. By this new iterative algorithm, the filter coefficients are quantized into optimal patterns which are favorable for the circuit implementation with significantly reduced area cost. The effectiveness of the proposed design algorithm is demonstrated using two design examples where the proposed design solution saves about 82.6% and 48.5% of hardware complexity over the baseline implementation and other competing methods.**

I. INTRODUCTION

Advanced digital signal processing methods and algorithms are intensively studied and applied to process electroencephalogram (EEG) signals measuring neuronal activity in the human brain. EEG signals can be captured by multiple-electrode EEG devices from inside the brain, over the cortex under the skull, or certain locations over the scalp [1]. Multi-layers structure in the human heads including the skull, scalp and brain are the major causes of the signal attenuation and noise generation. This yields to the great challenges in the EEG signal amplification and feature extraction. Therefore, development of efficient and precise electronic devices and processors to extract neuro-logical information from the brain EEG signals has become emerging research topics for clinical interests [1].

The typical EEG signal magnitude varies among 10–20 mV when measured from subdural electrodes and are subject to significant noise and artefacts. The artefacts, such as from the EEG − Functional Magnetic Resonance Imaging (fMRI) recording, significantly disturbs the EEG signals due to motion, gradient field, radio frequency, and cardiac cycle. [1]. To mitigate the noise and perform the spectral analysis along the low frequency range (<100 Hz) where neuronal information lies, digital filtering techniques such as a modulated filter bank are critical. Owing to the advantages of VLSI implementation, System-on-Chip (SoC) design by integrating the necessary and diverse EEG signal processing functions onto a low complexity chip becomes a cost and power efficient solution.

Many researchers have proposed approaches [3]-[6] to trade-off between filter coefficient precisions and the frequency response. [3]-[4] targeted at minimizing coefficients' wordlength by assuming that the actual hardware complexity is correlated with the coefficient wordlengths. [5] replaced low-amplitude coefficient's wasted digits in binary expression to improve the performance without increasing the wordlength. In fact, however, the filter complexity cost also significantly depends on the coefficients realization with the aids of logic operators reuse, such as coefficients commons subexressions sharing [7]. [6] did synthesis on the filter coefficients into a favorable set for the common subexpressions sharing, but the process deviated from the investigation of individual coefficient sensitivity to the quantization executed.

This paper will present a novel methodology to design effective digital filter bank with low silicon cost, dedicated to EEG signal extraction. To get to the root of the problem, the proposed method will address the challenges in synthesizing filter coefficients by accessing bit-level sensitivity and optimize logic operators sharing. This paper is organized as follows. Section II introduces the proposed coefficient sensitivity function and the adopted common subexpression statistics. Section III presents the proposed filter synthesis algorithm. It is followed by the design examples in EEG signal processor in Section IV and the conclusion is presented in Section V.

II. DEFINITIONS OF COMMON SUBEXPRESSIONS STATISTICS AND PROPOSED SENSITIVITY FUNCTION

A. Common Subexpressions and PT Array

By making use of the digit set $\{0, \pm 1\}$, a number can be represented as a sum of Signed-Power-of-Two (SPT) terms as in (1):

$$x = \sum_{i=0}^{W-1} s_i 2^i, s_i \in \{0, \pm 1\} \quad (1)$$

When the number of nonzero digits is minimal and the two

nonzero digits are never adjacent, the number can now be succinctly represented by a sequence of signed digits which is defined as Canonical Signed Digit (CSD) [8]. In our method, we synthesize our filter coefficients into CSD for its sparsity of representation and the minimal number of non-zero digits used. Any subexpressions with two non-zero digits at the two ends and a number of zero in between can be named as weight-two common subexpressions if they appear more than once in the coefficients set. To instantly keep track of the number of occurrence of subexpressions, we use the PT array of [9] defined as a 2×(w–2) dimensional array with the entry in the upper (lower) row and the j-th column represent the number of occurrences of positive (negative) subexpressions with j zeros between the two non-zero digits.

B. Frequency response and quantization error

For linear phase FIR filters with symmetric coefficients, its transfer function and frequency response $H(\omega)$ can be expressed as:

$$H\left(e^{j\omega}\right)=\sum_{i=0}^{N}h_i e^{-j\omega i} \tag{2}$$

$$H(\omega)=h(\frac{N-1}{2})+2\sum_{i=0}^{(N-1)/2-1}h(i)\cos((\frac{N-1}{2}-i)\omega) \quad N \text{ is odd} \tag{3}$$

$$H(\omega)=2\sum_{i=0}^{(N-1)/2}h(i)\cos((\frac{N}{2}-i)\omega) \quad N \text{ is even} \tag{4}$$

where N is the number of filter taps and ω is the frequency. The quantization error can then be defined as:

$$Q(\omega)=H(\omega)-\hat{H}(\omega) \tag{5}$$

where $H(\omega_i)$ and $\hat{H}(\omega_i)$ are the response before and after the quantization operation. In the application of EEG modulated Type-I FIR filters in [2], N is odd and hence equation (5) can be derived as

$$Q(\omega)=\left[h(\frac{N-1}{2})-\hat{h}(\frac{N-1}{2})\right]+2\sum_{i=0}^{(N-1)/2-1}\left[h(i)-\hat{h}(i)\right]\cos((\frac{N-1}{2}-i)\omega) \tag{6}$$

The stop-band attenuation, pass-band ripple and stop-band ripple are investigated before and after quantization through the coefficients synthesis process to keep them within accepted deviation.

C. Proposed Bit-level Sensitivity Function

The frequency response of a FIR filter is with different sensitivity to the coefficients, and actually varies for different bits within the same coefficients as well depending on the bit position. To guarantee the required specifications while keeping the synthesized CSD coefficients propitious to common subexpressions sharing, a bit-level sensitivity function to access impact on filter response by each non-zero digits in CSD representation is proposed, as:

$$S(h,m)=\frac{1}{K}\sum_{i=1}^{K}\left[H(\omega_i)-\hat{H}(\omega_i)\right]^2 \tag{7}$$

where m is representing the mth non-zero digit in the hth coefficient from left. K is the number of the frequency response samples used along the investigated frequency domain. $H(\omega_i)$ is the frequency response with the existing filter coefficients while $\hat{H}(\omega_i)$ is the response if the mth digit in hth coefficient is changed. Generally, with this sensitivity function, those more response-sensitive digits will be persisted even though they are not shared by any other subexpressions. Other digits which are not appearing in the common subexpressions are likely to be removed whenever sensitivities for these digits are sufficiently low.

III. Proposed Design Algorithm

A. Coefficients synthesis

The coefficients set are firstly generated by Matlab into infinite precision. We apply the traditional method in [10] to design the uniform statistical wordlength and quantized all the coefficients into finite precision at w-bit. Let δ_s and δ_p be the specified maximal acceptable deviations in the stop-band and pass-band, and ε_s and ε_p are the actual deviations from the ideal specification by the finite precision coefficients in stop-band and pass-band respectively. Heuristic algorithm with multiple constraints in such consideration is susceptible without appropriate initial conditions. Therefore, the w-bit original coefficients set h is firstly represented in CSD and the preliminary set P is produced by keeping only the Most Significant non-zero Digit (MSD) of each coefficient in h while eliminating all the rest. Those eliminated non-zero digits together with their parent coefficients index and bit location information are stored into the candidature set C. The preliminary set may not meet the required response specifications, so the compensation iteration starts to put back the necessary eliminated digits from C. Each digit in C is accessed by the proposed equation (7) to obtain its sensitivity. The digit with the highest bit level sensitivity, regardless of which coefficient it is from, is returned into its original position in its parent coefficient as in h. This produced the intermediate coefficients set which can be named as set I. Together with the MSD in the parent coefficient, the first returned digit can constitute the first subexpressions with two non-zero digits and hence the PT array is updated to record its existence. Because this subexpression will be realized by using one adder, the same subexpressions appearing in other coefficients can share this adder without extra cost. Therefore, the searching is executed in h and those digits in C who can build the same common subexpression are immediately shifted from C to I, followed by PT array and sensitivity data update. We access the quantization error and the algorithm moves on to search the next top sensitive digit if the error is still beyond the acceptable deviation δ_s and δ_p. The iteration continues until the desired specifications are met by coefficients set I.

The design procedure is summarized as the following pseudo code:

Coefficients_synthesis(h, δ_s, δ_p) {

Initialize P; // storage for coefficients with MSD only from h

```
    Initialize I=P;//storage intermediate coefficients through algorithm run
    C = h−P; //set for eliminated digits
    { ε_s , ε_p } = quantize(P);
    while ( ε_s > δ_s  or  ε_p > δ_p ) {
        n = sensitivity(C); // lookup for maximal sensitivity digit in C
        compensate(n, I);
        update(PT);
        m = search(h, PT);
        compensate(m, I);
        update(C);
        { ε_s , ε_p } = quantize(I);
    } // end of while loop
    return I;
}
```

Figure 1. Proposed coefficients synthesis algorithm

The function **quantize**(*I*) returns the stop-band and pass-band maximal deviations by the rounded coefficients set *I*. The function **sensitivity**(*C*) computes the sensitivity for each individual digit in *C* and returns the one with the biggest sensitivity. The function **search(***h***,**PT) searches the common subexpressions in *h* based on PT statistics and returns the digits *m* which can constitute common subexpression together with the existing digits in *I*. The function **compensate**(*m*, *I*) then moves the digit *m* from *C* to *I*. The key advantage of this algorithm is that the most sensitive digit is added back to compensate the response and the consequent common subexpression is immediately searched. Other digits who can utilize the sharing are added to further compensate the response without extra hardware cost. This way it will guarantee that the rounded coefficients set who can meet the specification is with very high likelihood of common subexpressions sharing in the subsequent filter circuit implementation.

B. Filter implementation with common subexressions

After the filter coefficients are designed and listed in set *I*, we can apply the following steps to design the multiplier block of the FIR filter with low adder cost.

Step 1: Look for the common subexpressions with the top frequency of occurrence in the final PT array generated in the coefficients synthesis process.

Step 2: Implement the subexpression using adder and shifters.

Step 3: Eliminating the implemented subexpressions from *I* and update PT array.

Step 4: Continue searching and elimination of common subexressions until no more left as indicated in PT array.

Step 5: Use additional adders to add the remaining SPT terms into the coefficients.

IV. Design Examples, Synthesis Results And Discussion

The first design example is the modulated filter bank consisting of seven Type I FIR filters employed in the EEG feature extraction processor [2]. Its filters specifications are given in Table II of [2] and sampling frequency is 75Hz after the decimation. These filters are firstly designed by using Chebyshev algorithm to generate infinite precision coefficients and quantized into 12-bit wordlength as original coefficients set in this example. The frequency responses of the designed filters BPF1 and BPF2 by direct implementation using the original coefficients set and by synthesized coefficients from the proposed algorithm are presented in Fig. 2 and Fig. 3, respectively. Because of the limited space, the frequency response diagrams for BPF3 to BPF7 are not presented, but the designed filter responses are carefully verified and they all meet the desired specifications. The filter circuits are then described in VHDL and mapped to 0.18μm CMOS standard cell library using Mentor Graphics LeonardoSpectrum™. The synthesized hardware costs measured by gate count in the standard cell are presented in Table I.

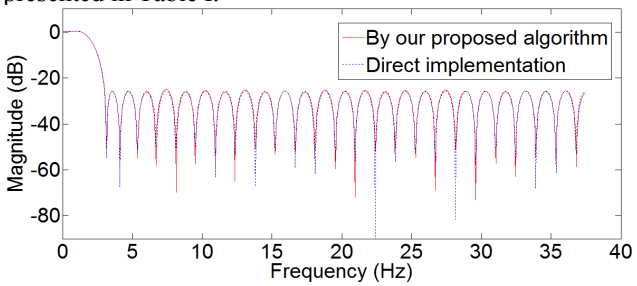

Figure 2. Frequency responses of the designed filter BPF1

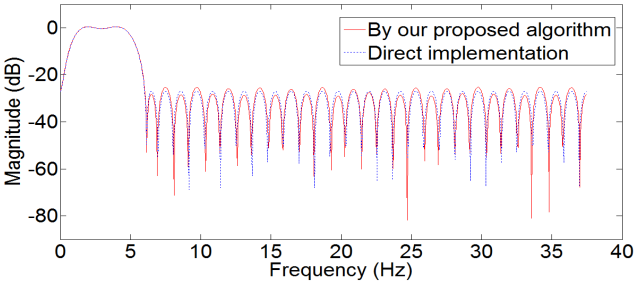

Figure 3. Frequency responses of the designed filter BPF2

TABLE I
Synthesized area cost of filters designed by direct implementation and the proposed algorithm for EEG filter bank

Filters	Direct Implementation	Proposed algorithm
BPF1	5016	1247
BPF2	5474	1285
BPF3	5955	806
BPF4	5190	867
BPF5	4554	717
BPF6	4852	627
BPF7	5021	718

From Fig. 2 and 3, our designed BPF1 and BPF2 are with very close frequency response as the filter designed by direct implementations. The stop-band attenuation of our designed filter is at 25dB. However, the hardware costs are saved by 75.1% and 76.5% respectively. From Table I, our proposed algorithm can design the EEG modulated filter bank with a total of 82.6% hardware cost reduction compared with the baseline direct implementation.

In design example 2, the proposed algorithm is applied to synthesized coefficients of the benchmark low pass filter presented in [3], with filter taps at *N*=67. The normalized pass-band and stop-band frequency are 0.2 and 0.3 respectively. The filter coefficients by [3], [4] and our method are listed in Table II. Their frequency responses are plotted in Fig. 4 by using Matlab Freqz function. The plotted

responses figures are verified using Matlab Filter Design & Analysis Tool. Assuming the input samples are with 8-bit wordlength, the synthesized hardware costs and delays by mapping to 0.18μm CMOS standard cell library are shown in Table III.

TABLE II
Designed filter coefficients by [3], [4] and the proposed algorithm

C	[3]	[4]	Proposed
h(34)	2^15-2^1	2^15	2^15
h(33, 35)	2^14+2^12+2^10-2^7+2^4-2^3-2^0	2^14+2^12+2^10-2^7+2^3+2^1	2^14+2^12+2^10-2^7
h(32, 36)	2^10-2^5+2^0	2^10-2^5	2^10-2^5
h(31, 37)	-2^13+2^11-2^9-2^7-2^5-2^3-2^1	-2^13+2^11-2^9-2^7-2^5-2^3-2^1	-2^13+2^11-2^9-2^7-2^5
h(30, 38)	-2^10+2^6+2^4+2^0	-2^10+2^6+2^4+2^1	-2^10+2^6+2^4
h(29, 39)	2^12-2^9+2^7+2^5+2^3	2^12-2^9+2^7+2^5+2^3	2^12-2^9+2^7+2^5
h(28, 40)	2^10-2^7-2^5-2^1	2^10-2^7-2^5-2^1	2^10-2^7-2^5
h(27, 41)	-2^10-2^8-2^5-2^3-2^1	-2^10-2^8-2^5-2^3-2^1	-2^11-2^8-2^6+2^4
h(26, 42)	-2^10+2^8+2^3	-2^10+2^8+2^3	-2^10+2^8
h(25, 43)	2^11-2^9-2^4+2^1	2^11-2^9-2^4+2^1	2^11-2^9
h(24, 44)	2^9+2^7+2^2	2^9+2^7+2^3-2^1	2^9+2^7
h(23, 45)	-2^10+2^5+2^2	-2^10+2^5+2^2	-2^10+2^5
h(22, 46)	-2^9-2^4+2^1	-2^9-2^4+2^1	-2^9-2^4
h(21, 47)	2^9+2^7-2^4	2^9+2^7-2^4	2^9+2^7-2^4
h(20, 48)	2^9-2^7+2^5-2^2-2^0	2^9-2^7+2^5-2^2-2^0	2^9-2^7+2^5
h(19, 49)	-2^9+2^7+2^2+2^0	-2^9+2^7+2^2+2^0	-2^9+2^7
h(18, 50)	-2^8-2^6+2^4-2^2+2^0	-2^8-2^6+2^4-2^1	-2^8-2^6+2^4
h(17, 51)	2^8-2^5-2^3-2^0	2^8-2^5-2^3	2^8-2^5
h(16, 52)	2^8-2^5-2^3	2^8-2^5-2^3	2^8-2^5
h(15, 53)	-2^7+2^4-2^0	-2^7+2^5	-2^7+2^4
h(14, 54)	-2^7-2^4-2^0	-2^7-2^5	-2^7-2^4
h(13, 55)	2^6-2^4+2^1	2^6-2^4+2^2	2^6-2^4
h(12, 56)	2^7-2^5-2^3	2^7-2^5-2^3+2^1	2^7-2^5
h(11, 57)	-2^4-2^1-2^0	-2^4-2^1	-2^4-2^1
h(10, 58)	-2^6+2^4-2^2+2^0	-2^6+2^4-2^2	-2^6+2^4
h(9, 59)	2^2-2^0	2^1	2^2-2^0
h(8, 60)	2^5-2^3+2^1	2^5-2^3+2^1	2^5-2^3
h(7, 61)	2^2-2^0	2^1	2^2-2^0
h(6, 62)	-2^3-2^1	-2^4+2^2	-2^4+2^2
h(5, 63)	-2^0	-2^2	-2^2+2^0
h(4, 64)	2^3-2^1	2^2	2^2
h(3, 65)	2^2	2^1	2^1
h(2, 66)	2^1	2^-4	0
h(1, 67)	0	-2^-2	0

TABLE III
Synthesized area cost and delay of benchmark filters

Algorithms	[3]	[4]	Proposed
Gate count	2437	1820	937
Delay (ns)	4.68	4.65	2.88

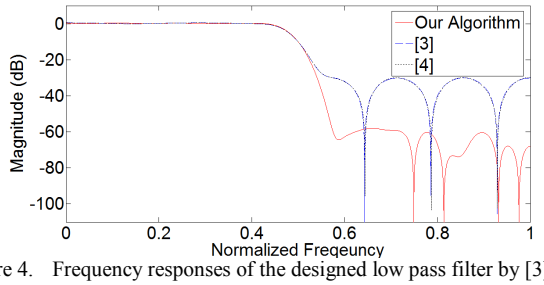

Figure 4. Frequency responses of the designed low pass filter by [3], [4] and our proposed algorithm

From Table II and Fig. 4, the response by [3] and [4] are almost overlapping while the proposed filter design can achieve the better stop-band attenuation by using less but more sensitive non-zero digits in the coefficients. Moreover, our synthesized coefficients are generated for better common subexpression sharing and hence the area cost can be significantly reduced. Our design has an area cost of 937 units, which is about 61.6% and 48.5% lower than [3] and [4]. The delay of our design also improves 38.5% and 38.1% over [3] and [4].

V. Conclusion

A new approach to the design of low complexity transposed direct form FIR filters is presented. A new sensitivity function is proposed to access the degree of influence on the filter response by every non-zero digits among the coefficients. By enhancing the common subexpressions sharing through the coefficients synthesis process, our method is applied to FIR filter bank in EEG signal processor with a significant implementation cost reduction at 82.6% compared with the baseline implementation. Applying the proposed algorithm to the benchmark filter design led to around 61.6% and 48.5% reduction in synthesized hardware complexity over competing methods. The proposed approach paves the way for efficient and accurate FIR filtering design with minimum hardware cost.

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