

Impact of Ionic Drift and Vacancy Defect Passivation on TDDB Statistics and Lifetime Enhancement of Metal Gate High- κ Stacks

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Abstract — Dielectric breakdown in high- κ gate stacks has been intensely studied over the past few years from an electrical, physical and statistical perspective. The mechanisms of stress induced leakage current (SILC) and subsequent time dependent dielectric breakdown (TDDB) as well as post-breakdown mechanisms in high- κ dielectrics have been relatively well understood now. Taking cue from the repeatable switching phenomenon in resistive random access memory (RRAM) devices, recent reports show that the percolative damage caused by TDDB and SBD is also partially recoverable. While electrical studies confirming SBD recovery are prevalent, the effect of this recovery on the statistics of the TDDB phenomenon has never been investigated. In particular, it would be useful to have a quantitative model to predict the lifetime enhancement for different degrees of recovery and estimate the role of recovery on the shape, convexity and Weibull slope of the breakdown distributions. Such a model can also be used to estimate the overall lifetime of the device for multiple recovery cycles and the role of gradually lowering efficiency in defect passivation as the device ages. We make use of the standard percolation cell framework here to examine the stochastics of recovery and subsequent breakdown events in pure high- κ dielectrics ignoring the presence of an intrinsic interfacial layer.

Keywords – Defect passivation, Ionic drift, Percolation, Recovery, Soft breakdown, Thermochemical model.

I. INTRODUCTION

With the advent of high- κ (HK) dielectrics replacing conventional SiON based technology, the statistical model and analysis methodology became very complex and non-idealistic due to various factors. Firstly, the high- κ HfO₂ layer most often became polycrystalline during deposition or annealing. As a result, the defect generation was preferentially localized in and around the grain boundary (GB) regions, as evidences from localized stress on blanket HK films using scanning tunneling microscopy (STM) [1, 2] and atomistic studies [3] have shown. The localization of defect generation and deviation from the random Poisson process induces a convexity to the failure distribution at low percentiles causing a deviation from the standard Weibull stochastics [4, 5]. Secondly, the presence of the sub-oxide interfacial layer (IL \rightarrow SiO_x) sandwiched between the high- κ and silicon substrate results in a dual-layer

dielectric stack. The stress experienced by the two dielectric layers has to be calculated using the Gauss law and the percolation process now happens in two stages, where after the first dielectric breaks down (SBD), there is an increase in the stress level across the second dielectric which subsequently percolates at a later time. The statistical formulation for such a scenario has to consider the time varying step-stress profile and using the cumulative damage model [6], the failure statistics of the HK-IL combination was derived, again with low percentile deviations [7]. Similar reports of non-Weibullian trends in high- κ stacks have been reported in Refs. [8] – [10].

The third scenario is where the percolation path could be partially repaired by applying a reverse polarity I - V sweep in the metal gate (MG)-HK stack. During the reverse sweep, the defects causing percolation are passivated and hence the percolation path is disconnected. Further finite duration stressing is needed to reform the path. This repair / recovery phenomenon derives its roots from the resistance switching process in RRAM non-volatile memory devices [11, 12] which have a similar stack as the transistor, except that the silicon substrate is replaced by a metal electrode (M-I-M capacitor). While some electrical studies have already confirmed the possibility of SBD recovery in MG-HK [13], the statistical implications of this phenomenon have not been dealt with.

If we were to practically utilize the SBD recovery concept in real circuits (using reverse I - V sweep circuit ‘*refresh*’ like ideology), then it becomes essential to statistically model the recovery phenomenon in terms of the probability of a certain number of defects that are annihilated and the new failure distribution for the subsequent stage of post-recovery stressing. The model we develop should enable us to estimate the lifetime enhancement we can achieve and predict the shape of the distribution and trend of Weibull slope variations for different degree of recovery. This study aims to accomplish this by building on our current 2D percolation cell framework that is well established to model defect generation in ultra-thin dielectric films [14, 15]. The generic thermochemical model [16] is used for characterizing field and temperature assisted defect generation rate (λ_G) here. The expression for λ_G can be modified if the role of carrier fluence needs to be included into the defect generation process. As for the rate of ionic drift /

diffusion, represented by λ_D , the Mott's ionic transport theory [17] is applied which considers drift as an additive directional mechanism to the standard diffusion process that can occur in any direction with different activation barriers.

The flow of this study is organized as follows. In Section II, we shall present electrical test results on the I - V trends of MG-HK stacks that clearly demonstrate the consistent bipolar recovery of leakage current after percolation. Section III presents the percolation framework and the statistical model used to describe the failure distribution for post-recovery TDDB, considering the stochastic nature of the location and count of traps that get passivated during the recovery I - V sweep. The results of the simulation in terms of the Weibull probability plots, considering the effect of diffusion barrier (E_{ad}) for ionic motion as well as the role of process induced defects and their competition with the recovered percolation column for subsequent breakdown are presented in Section IV. The influence of dielectric thickness and device area will also be considered. Finally, we conclude the study by postulating the mechanisms behind the limited number of repeated recovery events that constrain the application of the circuit reflash technique and propose ideas for further investigation.

II. ELECTRICAL EVIDENCE OF SBD RECOVERY

The soft breakdown and recovery tests were carried out on TiN – HfO₂ (1.8 nm) – Si NMOS stack devices with an almost zero interfacial layer. Breakdown was initiated using either constant or ramp voltage stress at $T = 298\text{K}$ with a very low compliance cap of $I_{comp} \sim 0.7\text{-}1\mu\text{A}$ corresponding to SBD and recovery (REC) was initiated using a slow negative ramp sweep from $0 \rightarrow -2.5\text{V}$ at a ramp rate of 100mV/sec . After every BD and REC event, the device transfer and drive current characteristics (I_d - V_g , I_g - V_g , I_d - V_d) were measured with reference to the fresh device.

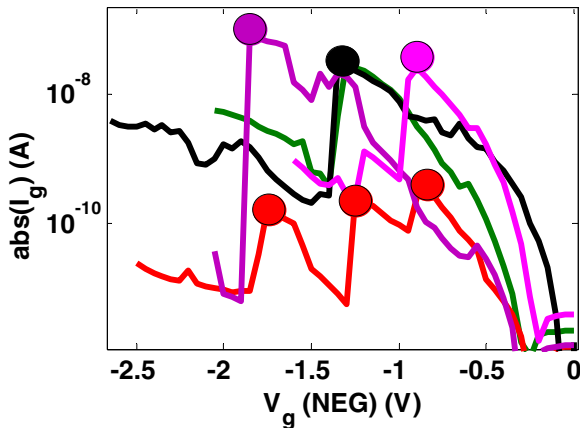


Figure 1. Recovery of leakage current during negative I_g - V_g sweep after SBD event showing multi-step drop in the current.

The significant drop in leakage current by 1-3 orders of magnitude is shown in Fig. 1 during the recovery sweep. Notice that recovery is a multi-step process involving discrete current jumps corresponding to individual V_0^{2+} : O^{2-} recombination events. When the I_g - V_g trends are measured after BD and REC, there is a clear gap in the leakage levels by around 1-2 orders of magnitude, as seen in Fig. 2. The

recovered state of the dielectric is quite stable with the noise appearing subdued because recovery is a chemical phenomenon ($O^{2-} + V_0^{2+} \rightarrow O_0$) that permanently passivates the oxygen vacancy defect, unlike a charge trapping process which is purely stochastic and the electron can be emitted again. The mechanism of recovery is illustrated by the schematic in Fig. 3 which is based on our physical evidence of oxygen vacancy being the fundamental constituent of the percolation path [18]. The metal electrode (TiN) serves as a very good oxygen reservoir and it is this property that enables the storage of O^{2-} ions in their mobile form in the electrode and their subsequent reverse drift when V_g polarity is reversed. In the case of poly-silicon gate technology, such recovery is seldom observed and not consistent as Si tends to get oxidized easily with very low oxygen solubility.

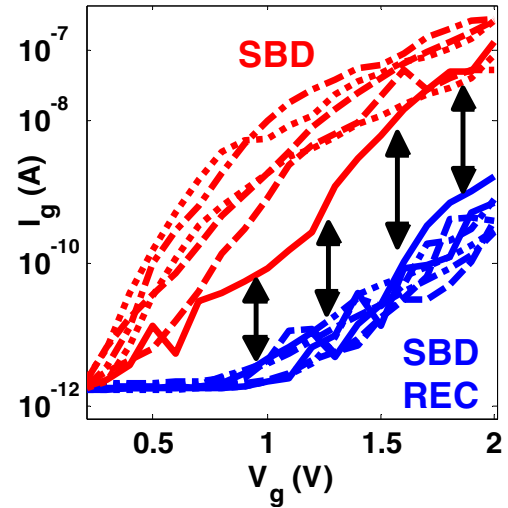


Figure 2. Observed I_g - V_g trends after SBD and REC for a single device over many cycles. There is a clear difference in the conductivity for the two states. The spread is higher in the SBD state due to random telegraph noise from percolated traps with large ΔI and probably coulomb blockade effect as well.

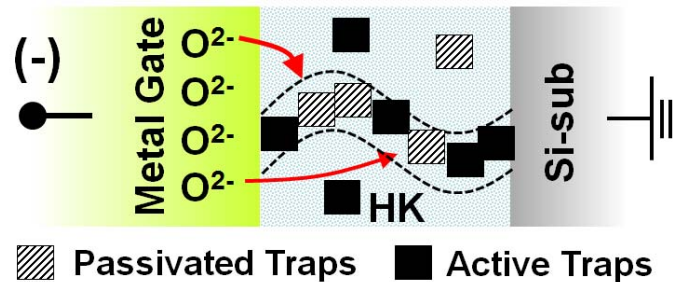


Figure 3. Mechanism of SBD recovery which involves passivation of the oxygen vacancy traps (defects) (represented by squares) by mobile oxygen ions that are stored in the metal electrode. These mobile ions drift to the electrode during TDDB stress when Hf-O bonds are broken and O^{2-} ions are liberated. They drift back to passivate the traps when a reverse bias is applied.

The lateral leftward shift in the transconductance peak after REC as compared to the trend after BD, extracted from the I_d - V_g transfer curve, is evident in Fig. 4. We also plot the zig-zag trends in the threshold voltage (V_{TH}) variation after BD and REC for many cycles on many similar devices in Fig. 5. The even numbers in the x -axis of the figure correspond to BD events and the odd numbers represent the recovered state. Clearly, in addition to the I_g level drop, we also see a

substantial improvement in the V_{TH} value whereby it tends back closer to the initial virgin device value after the percolation induced significant increase. This suggests that we can expect an enhancement in both the TDDDB and NBTI lifetimes after recovery. Some of the bulk defects and perhaps interface defects are also passivated during recovery that results in this rejuvenation of V_{TH} value.

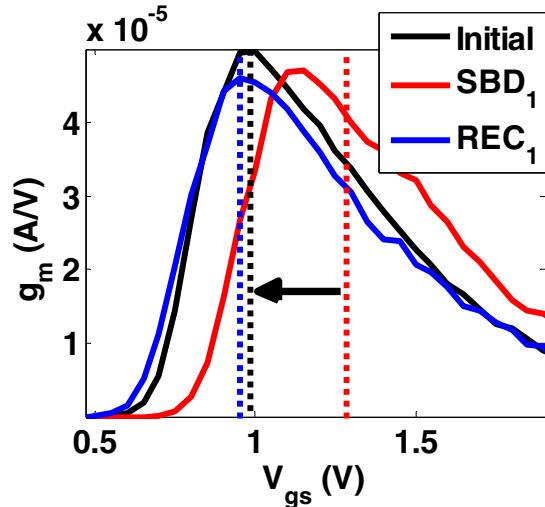


Figure 4. Shift in transconductance (g_m) of the NMOS device after SBD and subsequent recovery (REC), relative to the initial transfer characteristic.

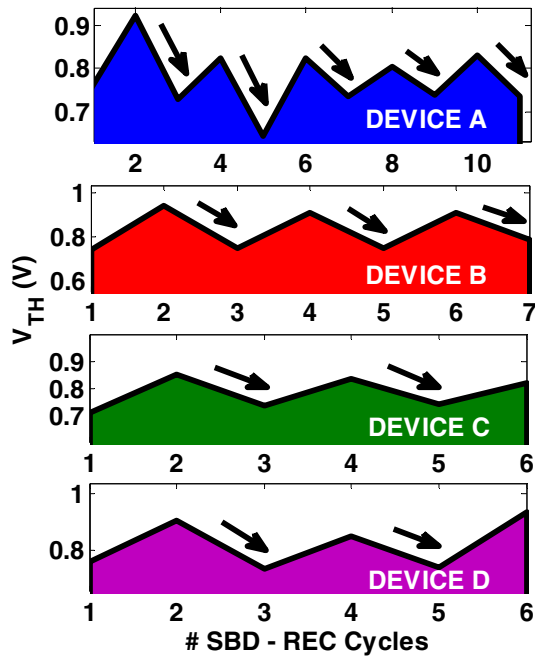


Figure 5. Zig-zag plot of the consistent increase and decrease in V_{TH} after SBD and REC respectively for many cycles in four different devices. Every upward shift in V_{TH} corresponds to SBD and downward shift is for REC.

In Fig. 6, we plot the random telegraph noise (RTN) trends in two similar devices sensed at $V_g = 1.25V$ after SBD and after subsequent recovery. The current step in the RTN signal drops from $\Delta I \sim 1-50nA$ all the way down to $\Delta I \sim 5-50pA$, which is a shift of around 2-3 orders of magnitude. The RTN trends seldom disappear after recovery because there are still

disconnected defects as well as process induced defects where RTN can continue to occur, though the absolute value of the signal drops to pico-ampere range due to long tunneling distance without any trap clusters.

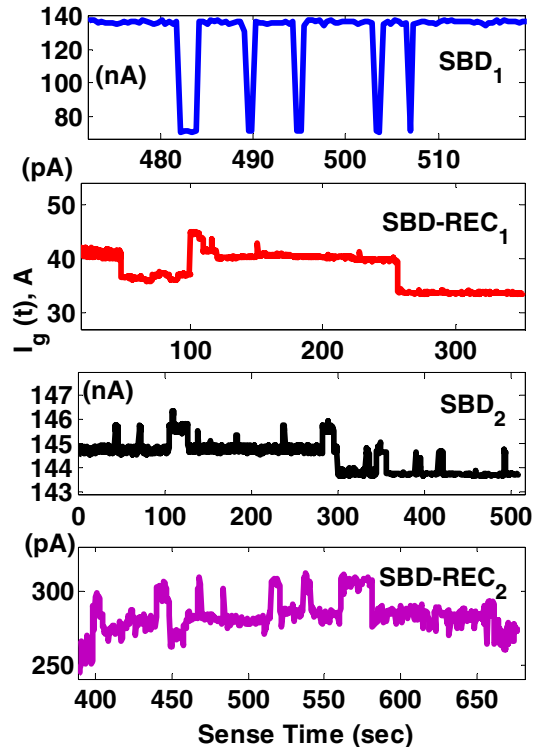


Figure 6. RTN signal sensed at $V_g = 1.25V$ in two devices for a cycle of SBD and REC. The value of ΔI is orders of magnitude different after SBD and REC indicating that recovery is a stable defect passivation phenomenon.

III. MODEL FOR POST-RECOVERY BREAKDOWN

The 2D cell framework used to model the nucleation and rupture of the percolation path is shown in Fig. 7. For the very first TDDDB event, the standard expressions for failure probability can be developed considering the defect generation rate (λ_G), expressed by Eqn. (1) [16] and the corresponding time-dependent probability expression (p_{GEN}) given by Eqn. (2), where E_{aG} , p_0 , κ , v and ξ refer to the field-free bond activation energy, dipole moment, relative permittivity, lattice vibration frequency and electric field respectively.

$$\lambda_G = v \cdot \exp\left(-\frac{E_{aG} - p_0 \cdot (2 + \kappa) / 3 \cdot \xi}{k_B T}\right) \quad (1)$$

$$p_{GEN}(t) = 1 - \exp(-\lambda_G \cdot t) \quad (2)$$

As for the recovery stage, it is in fact a two-stage process involving first the drift / diffusion of oxygen ions from the gate electrode into the dielectric across a potential interface barrier and the subsequent recombination of the defects which is a chemical reaction ($O^{2-} + V_o^{2+} \rightarrow O_o$). The rates for the drift and recombination are represented by λ_D and λ_{REC} [19], which can be expressed by Eqns. (3) and (4) respectively where x is the average drift distance, a is the atomic spacing (lattice periodicity), E_{aD} is the diffusion activation barrier and E_{aR} is

the activation energy for recombination to take place (typically $E_{ar} \ll E_{ad}$). We consider recovery to be equally feasible for all the traps in the percolation path, independent of their distance from the electrode interface as a first order approximation.

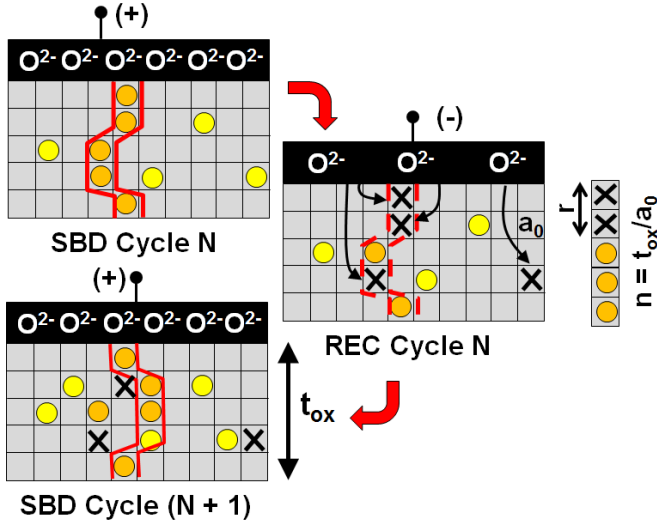


Figure 7. Percolation schematic used to describe partial recovery and subsequent breakdown events in the high- κ stack. Depending on the extent of recovery, area of the device and process induced defect density, the location of next BD event after REC can be correlated – uncorrelated. The yellow and orange circles here represent process and stress-induced defects respectively. The symbol 'X' refers to locations where the defect was passivated.

$$\lambda_D = \frac{\nu}{x} \cdot a \cdot \exp\left(-\frac{E_{ad}}{k_B T}\right) \cdot \sinh\left(\frac{qa\xi}{2k_B T}\right) \quad (3)$$

$$\lambda_{REC} = \nu \cdot \exp\left(-\frac{E_{ar}}{k_B T}\right) \quad (4)$$

Using a two-step sequential Markovian formulation for the recovery process which involves ionic drift followed by chemical recombination, the overall recovery probability ($p_{REC}(t)$) can be expressed by Eqn. (5) as a function of time. For the case of post-recovery breakdown, the reliability function can be expressed by Eqn. (6) as a series product of the reliability of the single recovered percolation column (R_{PERC}) and the reliability of the remaining ($N-1$) unpercolated columns ($R_{UN-PERC}$), where N is the number of columns in the cell-based construct that represents the area of the device in a 2D plane.

$$p_{REC}(t) = 1 - \frac{1}{1 - \lambda_{REC}/\lambda_D} \cdot e^{-\lambda_{REC}t} + \frac{1}{\lambda_D/\lambda_{REC} - 1} \cdot e^{-\lambda_D t} \quad (5)$$

$$R_{BD}(t) = R_{PERC}(t) \cdot R_{UN-PERC}(t) \quad (6)$$

The expression for R_{PERC} is given in Eqn. (7) where the reliability of the recovered path depends on the number of passivated defects (r) during the previous recovery cycle. This number is purely stochastic and could range anywhere between $r = 0$ to $r = n = t_{ox}/a_0$ where t_{ox} is the dielectric thickness and a_0 is the trap size. The stochastics of r can be modeled using the

discrete binomial distribution function to estimate the probability of a certain number of defects being passivated given the voltage and time duration pulsing conditions for recovery (V_{REC}, t_{REC}). As for the unpercolated regions, where it is possible for the next percolation to occur when the current breakdown path is sufficiently well passivated and also with the area effect coming in (many unpercolated columns exist where one of them could potentially break), the expression for $R_{UN-PERC}$ is given by Eqn. (8).

$$R_{PERC}(t) = \sum_{r=0}^n (1 - p_{GEN}^r) \cdot B(n, r) \quad (7)$$

$$= \sum_{r=0}^n (1 - p_{GEN}^r) \cdot [p_{REC}^r \cdot (1 - p_{REC})^{n-r} \cdot {}_r C^n]$$

$$R_{UN-PERC}(t) = (1 - p_{GEN}^{n-PIT})^{N-1} \quad (8)$$

Using the above percolation framework, we shall now simulate the failure distribution plots, investigating various factors such as probability of recovery (depends on E_{ad}), dielectric thickness, area and the role played by process induced traps.

IV. STATISTICAL SIMULATIONS OF POST-RECOVERY SUBSEQUENT BREAKDOWN EVENTS

A. Role of Process Induced Traps on Virgin Device TDDB

Prior to analyzing the post-recovery influence on the statistics, we first simulate the distribution of TDDB lifetime for the very first breakdown, assuming different average number of process induced traps (PIT) in Fig. 8 for $n = 7$ rows, corresponding to a physical thickness of $t_{ox} \sim 5.6$ nm (if we assume $a_0 \sim 8\text{\AA}$) and $V_{stress} = 2V$. It is to be noted that the distribution plot is very convex for low values of PIT with a steep Weibull slope (β) value in the low percentile range. With higher PIT, the slope becomes shallower and the β values in the low and high percentile range are almost close to each other. We can infer that the low percentile slope (β_{LP}) scales well with PIT, while for high percentile (β_{HP}), the slope is relatively independent of the PIT density.

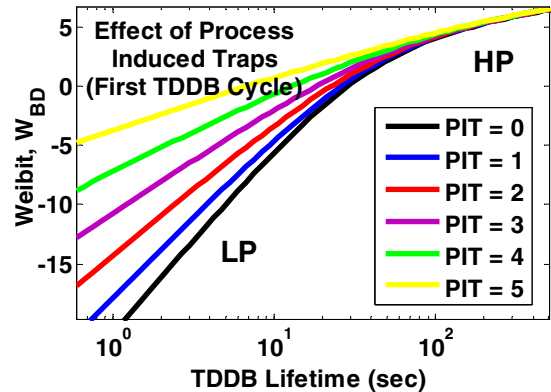


Figure 8. Distribution of the first BD time for $n = t_{ox}/a_0 = 7$ with the presence of different number of (average) PIT in every column of the dielectric.

B. Role of Defect Recovery Probability on Subsequent TDDB

The trend of β_{LP} with p_{REC} and the enhancement in breakdown lifetime (relative to the first TDDB event) for different p_{REC} is plotted in Figs. 9(a) and 9(b) respectively. We observe a clear reduction in the β_{LP} value for poor recovery as the number of additional defects needed to percolate the column is lower. We desire to have a high β so that the variability issues can be minimized. For $p_{REC} = 50\%$, the percentage enhancement in mean TDDB lifetime is computed to be around 30%. We plot the shape of the failure distribution for different values in the range of $p_{REC} \in (5\% - 100\%)$ for $\{V_{stress} = 2V, V_{REC} = -1V\}$ in Fig. 10. As p_{REC} decreases, the LP bend in the non-Weibull distribution shifts from “convex” to “concave” and becomes flatter. This implies there is a drastic increase in spread of failure time when recovery is ineffective.

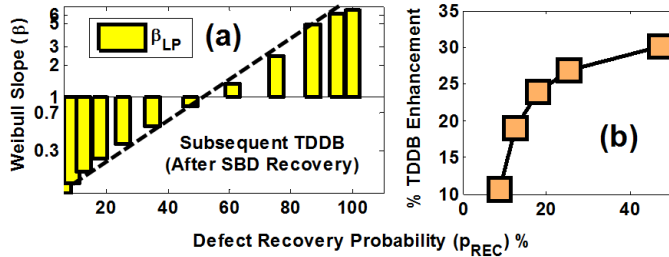


Figure 9. (a) Variation of β_{LP} for different p_{REC} . (b) Trend of percentage enhancement in mean time to failure (scale factor) for different p_{REC} . The value of p_{REC} has the biggest impact in the LP regime as evident in Fig. 10.

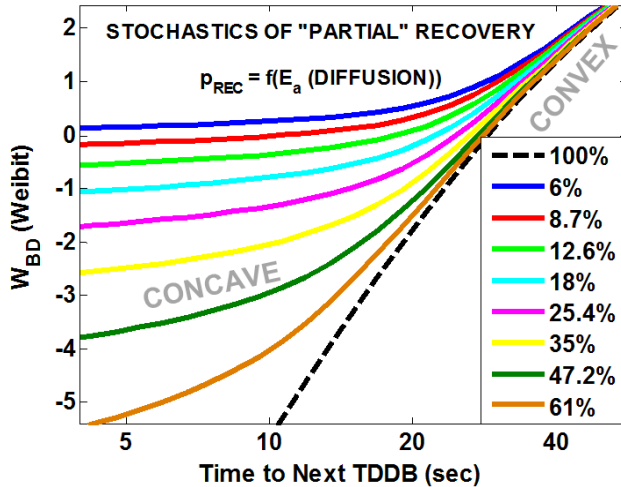


Figure 10. Observation of the concave bend in the failure distribution for BD after partial recovery of percolation path ($t_{ox} = 4$ nm). The concavity increases as defects become more difficult to passivate. The distribution is “fully convex” only for the ideal case of complete recovery. Note that p_{REC} is changed by modifying the value of E_{ad} , the key determinant for recovery.

C. Role of Dielectric Thickness

The simulated distribution of next breakdown time as a function of physical dielectric thickness is plotted in Fig. 11, keeping p_{REC} fixed at 35% and considering a normalized ξ -field (by adjusting the stress / recovery voltage for different t_{ox}) for a clear comparison. It is evident that the flat bending of the distribution curve begins at much lower percentiles for thicker dielectrics. This is logically expected because there is a higher

probability of at least one defect recovery given the larger number of available $V_0^{2+} - O^{2-}$ complementary pairs.

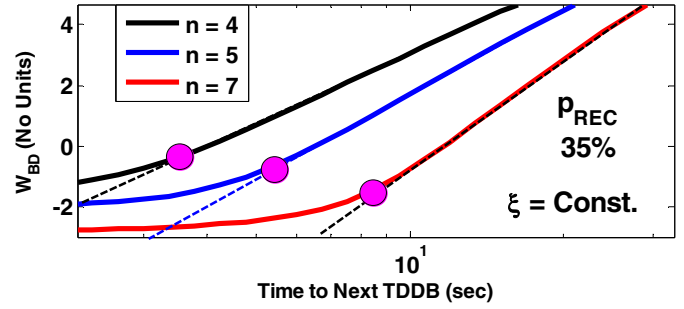


Figure 11. Weibull trend of next time to BD as a function of the dielectric thickness for a constant ξ -field and $p_{REC} = 35\%$.

D. Correlated – Uncorrelated Location of Next BD Event

The role of initial defectivity in the dielectric and the percolation recovery probability on the correlation of the BD spot location for different BD events during repeated BD-REC cycles is exemplified by the Weibull plot in Fig. 12. As the PIT density increases, the distribution curve returns back from a concave shape to the standard convex trend because the recovered percolation path and other unpercolated columns tend to have almost the same number of defects to be generated for a percolation to occur again. As a result, there is lower dominance of the recovered percolation path and the BD events during multiple cycles tend to be increasingly uncorrelated as the PIT density increases.

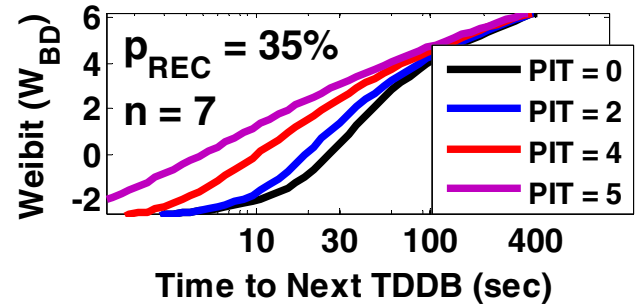


Figure 12. Weibull trend for time to next BD in a recovered percolation path shows that in the presence of high PIT all over the dielectric, the degradation is more uniform and the failure distribution trend returns to the conventional “convex” pattern (refer to curve for PIT = 5).

E. Area Scaling Trends for Recovered Dielectric

In Fig. 13, the next BD time distribution plot compares the trend for three device areas that are one order of magnitude different from each other. Notice that the concavity exists only for the very small area devices, while for larger area structures, there is a high chance of percolation occurring elsewhere in the unpercolated columns due to dominance of areal degradation. Therefore, area scaling rule tends to become increasingly valid (in an approximate sense) as the area of the device is increased.

F. Decoding the Overall Failure Distribution

Based on the analysis thus far, it is clear that the overall failure distribution for the recovered dielectric depends on four key factors \rightarrow (a) probability and extent of recovery (E_{ad}

value), (b) spatial density and distribution of PIT in the virgin device (some of which could also arise during SILC stage as well), (c) area of stack and (d) physical thickness of dielectric. In order to explicitly observe the contributions to the shape of the overall distribution from the recovered region and the remaining unpercolated region of the device, we plot the overall cumulative failure function as well as the failure probability for the percolated (Eqn. 7) and unpercolated columns (Eqn. 8) separately in Fig. 14 for $p_{REC} = 25\%$, 35% and 47% arbitrarily. It is worth noting that the unpercolated region (red line) is almost perfectly Weibull with some slight convexity and steep slope, which is the traditional shape of the distribution we would expect. The contribution from the recovered percolation path (blue lines) has a very shallow β and it is the only one that contributes to the concavity at low percentiles. The intersection of the blue and red lines (represented by yellow dots) is the cross-over point for the dominance of different regions in the overall breakdown process. As we go to lower percentiles, the partially ruptured percolation path dominates the next BD trend; while for higher percentiles, the unpercolated region contributes to the shape of the distribution. The cross-over point logically shifts downward as the value of p_{REC} gets higher. Note that the black lines in Fig. 14 represent the overall distribution, according to Eqn. (6).

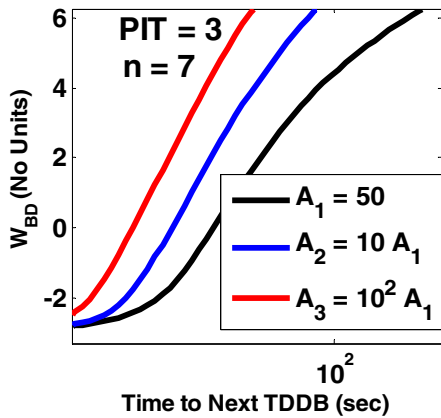


Figure 13. Trend of decreasing concavity as the device area gets larger because the areal degradation tends to dominate over the local degradation (for the next BD event) in the recovered percolation path.

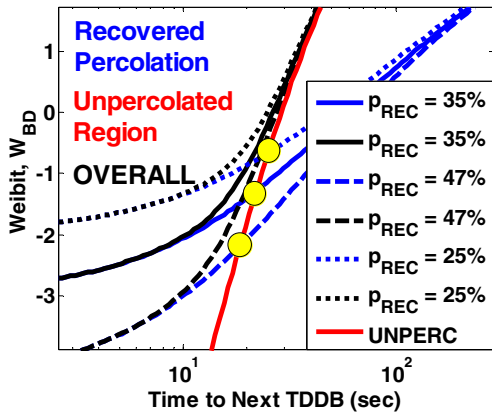


Figure 14. Weibull plot for different p_{REC} showing overall failure distribution (black lines) tends towards the recovered percolation column (blue lines) for low percentile and areal unpercolated region (red line) for high percentile.

V. CONCLUSION

In this study, we examined in detail the influence of the soft breakdown recovery process on the statistical distribution for the subsequent time to BD, accounting for non-ideal factors of incomplete recovery and process induced defect density. There is a significant difference in the shape of the distribution and the Weibull slope as well when comparing the BD of a virgin device with that of a recovered device. The partial recovery (ruptured oxygen vacancy filament) phenomenon induces a concave bend in the distribution for low percentile values which results in shallow β values (large spread in BD distribution). The change in shape of the distribution for different dielectric thickness and device area was also examined. The concavity is less evident for thicker dielectrics and area scaling becomes increasingly valid for larger area devices even for the partially recovered stacks. The main objective of this investigation was to highlight the deviations in the statistical distribution when recovery is accounted for and to build upon the existing percolation based cell construct to describe the SBD recovery phenomenon and quantify the lifetime enhancement it can provide. The statistical model here has to be further fine-tuned and fit to experimental test data on repeated post-recovery TDDB tests so as to extract the values of E_{ad} , E_{ar} and E_{ag} and estimate accurately the remaining useful life distribution of the transistor for any given scheme of pre-programmed circuit reflash technique (set of values of recovery pulse voltage, duration and frequency) as shown in Fig. 15(a).

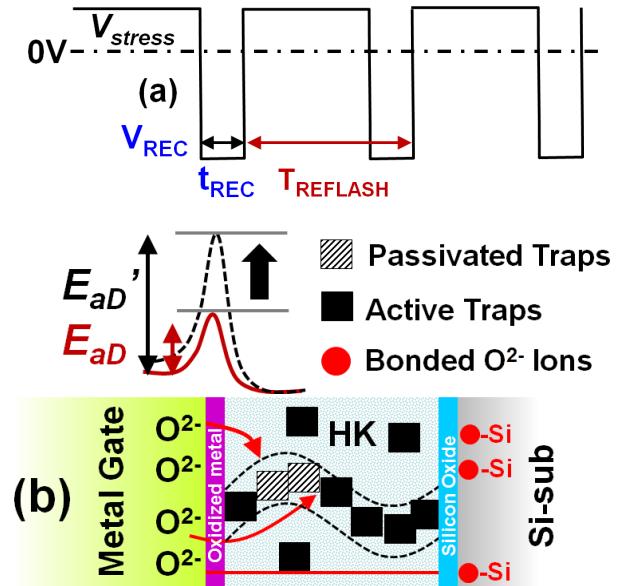


Figure 15. (a) Circuit reflash algorithm that could be programmed so as to initiate bipolar pulses at a certain frequency with amplitude V_{REC} and pulse duration t_{REC} . The value of V_{REC} and / or t_{REC} may have to be increased as the device ages or the frequency of reflash actions ($f = 1/T_{REFLASH}$) should be increased. (b) Schematic illustrating increasing imbalance in mobile O^{2-} and immobile V_O^{2+} count due to oxidation of metal electrode and / or silicon substrate, thereby gradually limiting the recovery phenomenon ($E_{ad}' > E_{ad}$).

Note that the SBD recovery process has its own limitations. Firstly, there is a thermodynamic and kinetic limit to the

number of recovery events that can take place. This is because the oxygen ions could eventually oxidize the metal gate electrode (forming a metal oxide barrier, which increases the migration barrier, E_{ad} , for remaining O^{2-} ions further). Secondly, some oxygen ions during recovery could drift all the way to the Si-substrate and get oxidized there too. As a result, there is an increasing imbalance in the $O^{2-} - V_0^{2+}$ count which makes recovery progressively less effective (refer to Fig. 15(b) which illustrates these phenomena). Lastly, the SBD recovery we discuss here is only applicable to NMOS devices because the inversion stress (positive polarity) enables negatively charged oxygen ions to drift to the metal gate and return back easily. If we were to consider the PMOS device, the inversion is at negative polarity which causes liberated O^{2-} ions to drift towards the silicon substrate, where they most likely get oxidized (as Si has very poor oxygen solubility of 0.004 at % as compared to Ti with 33 at %) [13]. If applying a reflash recovers only defects in NMOS, but not in PMOS, the circuit variability becomes worse (although reliability is improved), which may not always be desirable. This reliability – variability trade-off at the circuit level deserves further study.

As shown earlier in Ref [20], SBD recovery gradually degrades with many cycles of bipolar $I-V$ sweeps, as the imbalance between O^{2-} and V_0^{2+} increases. Therefore, there is a limit to how many reflash attempts would be effective at the circuit level. Our focus thus far has been on the standard Si-based logic technology only. It would be useful if attempts to recover the breakdown event are investigated in III-V (GaAs, InP) based high power – high mobility gate stacks as well so that the feasibility of this phenomena in non-Si substrate based stacks could be assessed. Given that III-V based stacks currently suffer from various reliability issues that are yet to be solved, SBD reversibility could come in handy in boosting the front-end device lifetime of these new technologies.

ACKNOWLEDGMENT

The authors would like to thank the International Design Center (IDC) at the Singapore University of Technology and Design (SUTD) for fully funding this research work and provision of the travel allowance under Grant No. IDG11300103.

REFERENCES

[1] K. Shubhakar, K.L. Pey, S.S. Kushvaha, S.J. O’Shea, N. Raghavan, M. Bosman, M. Kouda, K. Kakushima and H. Iwai, “Grain boundary assisted degradation and breakdown study in cerium oxide gate dielectric using scanning tunneling microscopy”, *Applied Physics Letters*, Vol. 98, No. 7, 072902, (2011).

[2] Y.C. Ong, D.S. Ang, K.L. Pey, S.J. O’Shea, K.E.J. Goh, C. Troade, C. H. Tung, T. Kawanago, K. Kakushima and H. Iwai, “Bilayer gate dielectric study by scanning tunneling microscopy”, *Applied Physics Letters*, Vol. 91, No. 10, 102905, (2007).

[3] K. McKenna and A. Shluger, “The interaction of oxygen vacancies with grain boundaries in monoclinic HfO_2 ”, *Applied Physics Letters*, Vol. 95, No. 22, 222111, (2009).

[4] N. Raghavan, K.L. Pey, K. Shubhakar, X. Wu, W.H. Liu and M. Bosman, “Role of grain boundary percolative defects and localized trap

generation on the reliability statistics of high- κ gate dielectric stacks”, *IEEE International Reliability Physics Symposium (IRPS)*, pp.6A.1.1-6A.1.11, (2012).

[5] N. Raghavan, K.L. Pey, K. Shubhakar and M. Bosman, “Modified percolation model for polycrystalline high- κ gate stack with grain boundary defects”, *IEEE Electron Device Letters*, Vol. 32, No. 1, pp. 78-80, (2011).

[6] W. Nelson, “Accelerated Testing: Statistical Models, Test Plans and Data Analyses”, *John Wiley & Sons*, (1990).

[7] N. Raghavan, K.L. Pey, W.H. Liu, and X. Li, “New statistical model to decode the reliability and weibull slope of high- κ and interfacial layer in a dual layer dielectric stack,” *IEEE International Reliability Physics Symposium (IRPS)*, pp. 778-786, (2010).

[8] T. Nigam, A. Kerber, and P. Peumans, “Accurate model for time-dependent dielectric breakdown of high- κ metal gate stacks”, *IEEE International Reliability Physics Symposium (IRPS)*, pp. 523-530, (2009).

[9] E.Y. Wu, J. Suñé and C. LaRow, “Generalized successive failure methodology for non-weibull distributions and its applications to SiO_2 or high- κ / SiO_2 bilayer dielectrics and extrinsic failure mode”, *IEEE International Reliability Physics Symposium (IRPS)*, pp. 6A.2.1-6A.2.7, (2012).

[10] R. Foissac, S. Blonkowski, M. Kogelschatz, P. Delcroix, M. Gros-Jean and F. Bassani, “Impact of bilayer character on high- κ gate stack dielectrics breakdown obtained by conductive atomic force microscopy”, *Microelectronics Reliability*, Vol. 53, No. 12, pp.1857-1862, (2013).

[11] K.L. Pey, N. Raghavan, X. Wu, W.H. Liu and M. Bosman, “Dielectric breakdown—Recovery in logic and resistive switching in memory— Bridging the gap between the two phenomena”, *11th International IEEE Conference on Solid-State and Integrated Circuit Technology (ICSICT)*, pp. 1-6, (2012).

[12] E. Miranda, D. Jimenez and J. Suñé, “From post-breakdown conduction to resistive switching effect in thin dielectric films”, *IEEE International Reliability Physics Symposium (IRPS)*, pp. GD.5.1-GD.5.6, (2012).

[13] N. Raghavan, K.L. Pey, X. Wu, W.H. Liu, X. Li, M. Bosman and T. Kauerauf, “Oxygen-soluble gate electrodes for prolonged high- κ gate stack reliability”, *IEEE Electron Device Letters*, Vol. 32, No. 3, pp.252-254, (2011).

[14] J.H. Stathis, “Percolation models for gate oxide breakdown”, *Journal of Applied Physics*, Vol. 86, No. 10, pp.5757-5766, (1999).

[15] J. Suñé, “New physics-based analytic approach to the thin-oxide breakdown statistics”, *IEEE Electron Device Letters*, Vol. 22, No. 6, pp.296-298, (2001).

[16] J.W. McPherson, R.B. Khamankar and A. Shanware. “Complementary model for intrinsic time-dependent dielectric breakdown in SiO_2 dielectrics”, *Journal of Applied Physics*, Vol. 88, No. 9, pp. 5351-5359, (2000).

[17] D.B. Strukov and R.S. Williams, “Exponential ionic drift: fast switching and low volatility of thin-film memristors”, *Applied Physics A*, Vol. 94, No. 3, pp.515-519, (2009).

[18] X. Li, C. H. Tung, K. L. Pey and V. L. Lo, “The chemistry of gate dielectric breakdown”, *IEEE International Electron Devices Meeting (IEDM)*, pp. 1-4, (2008).

[19] S. Yu, Y.Y. Chen, X. Guan, H.S.P. Wong and J.A. Kittl, “A Monte Carlo study of the low resistance state retention of HfO_2 based resistive switching memory”, *Applied Physics Letters*, Vol. 100, No. 4, 043507, (2012).

[20] N. Raghavan, K.L. Pey, W.H. Liu, X. Wu, X. Li and M. Bosman, “Evidence for compliance controlled oxygen vacancy and metal filament based resistive switching mechanisms in RRAM”, *Microelectronic Engineering*, Vol. 88, No. 7, pp.1124-1128, (2011).