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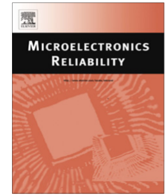

Variability model for forming process in oxygen vacancy modulated high-κ based resistive switching memory devices

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ABSTRACT

Forming is one of the key phenomenon that governs the subsequent switchability in high-κ based resistive random access memory (RRAM) devices. The variability of subsequent switching events (voltage and resistance state), shape and size of filament, reliability of the non-volatile memory device in terms of endurance and retention as well as ultra-low power operation of the memory array all depend on the forming process in one way or the other. As a result, controllability of forming and reduction of the forming voltage is an important design activity in the RRAM technology development process. In this study, we analyze the various factors that affect the forming voltage distribution from a simulation perspective using a Kinetic Monte Carlo (KMC) based formulation of the vacancy defect evolution process in the dielectric. The impact of high-κ microstructure (grain boundaries), metal–oxide interface roughness, deposition process induced defect distribution as well as role of multi-layer dielectric films on the forming time and spread is investigated in detail. The results of the study provide guidelines for further reliability design initiatives in tightening the forming distribution.

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1. Introduction

With advancements in data storage research and the need for aggressive downscaling of non-volatile memory (NVM) technology, reliability is becoming a show-stopper for Flash technology [1,2]. For a NAND flash cell, the difference between the binary '0' and '1' state for 60 nm node is governed by only around 67 electrons [3]. This implies that the charge loss of a few electrons can impact the memory window and threshold voltage variability to a large extent. The need for more stable memory states in small area devices brought about the evolution of the resistive random access memory (RRAM) where the switching between binary resistance states is governed by more robust defects such as oxygen vacancies [4] and/or metallic filaments [5], with the phenomenon being localized rather than device area dependent as is the case with Flash memory.

With the advent of RRAM and its evident robust performance metrics, reliability and variability of the device still remains a major issue that is being investigated in-depth by various research groups. In particular, the specific issues that need to be solved are controllability of forming [6], enhancement of endurance cyclability [7,8] and retention lifetime [9] as well as making the device immune to disturb events at read conditions of $V_{TE} = 100$ mV [10], where TE refers to the top electrode in the metal–insulator–metal (MIM) stack. The intrinsic physical phenomena governing the reliability and variability issues have to be better understood before we could provide design initiatives to enhance the reliability of this memory technology.

Our focus in this study is to simulate the forming process and investigate the various material/process factors influencing the spread in the forming time/voltage distribution. We shall consider the (a) role played by high-κ dielectric microstructure comparing amorphous and polycrystalline oxide films where grain boundaries are known to be the preferred weakest link paths for filaments to nucleate [11], (b) effect of the interface roughness between the metal electrodes and the dielectric, (c) role of physical sputtering induced random defect distribution in the virgin device and (d) impact of adopting a two-stage deposition process for high-κ so that the grain boundaries (GB) are misaligned [12]. We shall consider HfO_2 as the dielectric of interest here as it is one of the most potential candidates being considered for RRAM application and is compatible with the CMOS process as well. The switching mechanism of interest here is oxygen vacancy and oxygen ion transport, which is prevalent in the low power switching regime when the forming compliance is kept relatively low within 10–50 μA.

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2. Methodology of forming simulation

The forming process is simulated using the percolation framework that has been widely used to describe dielectric breakdown in logic gate stacks [13,14]. We construct a 2D cell-based percolation model as shown in Fig. 1. Every cell is associated with a defect generation rate (λ) and some of the columns are represented as grain boundaries (GB) with a higher value of λ that arises due to higher local relative permittivity at GB locations due to increased oxygen deficiency [15]. We simulate the forming process for t_{ox} ~ 2.4 nm, 3.6 nm and 4.8 nm, considering a defect size of $a_0 \sim 8$ Å [16]. The standard Monte Carlo procedure is implemented where the next location of defect evolution is chosen based on a random number generator, considering the weightage of the λ values at the grain and GB locations. In other words, the Monte Carlo routine automatically assigns a higher probability for defect nucleation to the GB sites. For a detailed outlook into the KMC procedure, readers can access Ref. [17].

The expression for λ can be given by Eq. (1) using the thermochemical model [18], where E_{aG} is the field-free bond activation energy (~4.4 eV for HfO_2 [19]), p_0 is the permanent dipole moment (10.2 eÅ [20]), κ is the permittivity, ν is the vibration frequency, ξ is the electric field and T is the Kelvin temperature. The value of κ for HfO_2 is typically ~25, but the local κ value is chosen to be higher around the GB, ranging between 25 and 28 due to higher density of oxygen vacancy. We shall discuss the role of the dielectric microstructure in the next section.

$$\lambda_G = \nu \cdot \exp\left(-\frac{E_{aG} - p_0((2+\kappa)/3)\cdot\xi}{k_B T}\right) \quad (1)$$

3. Microstructure impact on forming distribution

Various physical analysis studies based on localized stressing on blanket high-κ films [11,21] using the scanning tunneling microscopy (STM) and conductive atomic force microscopy (CAFM) techniques have revealed that the filament is more prone to nucleate at the GB location. Furthermore, atomistic studies point to the tendency of vacancies to thermodynamically migrate from the grain region and segregate at the GB junctions [22]. Assuming the Weibull distribution to hold true for forming (given that it is analogous to dielectric breakdown), Fig. 2(a) plots the distribution of forming time (t_{FORM}) for two different λ_{GB}:λ_G ratios of 2:1 and 16:1. It is evident that the distribution becomes increasingly convexial as the ratio increases, suggesting a deviation from Weibull stochastics because defect generation is increasingly localized and does not obey the spatially random Poissonian process anymore. In Fig. 2(b), the t_{FORM} distribution at the grain (G) and GB locations are extracted from a simulation of 1000 trials and plotted separately. As expected, it takes longer to form at grain locations and the distribution is closer to Weibull. On the contrary, forming is easier or faster at GB sites with a convexial deviation from the Weibull model at low percentiles.

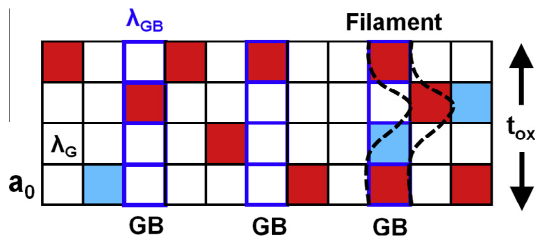

Fig. 1. Cell-based percolation construct to simulate the filament nucleation process in the polycrystalline high-κ dielectric with GB represented by the blue outlined columns. The cells shaded in blue and red refer to the process-induced and stress-induced vacancies and a certain pattern of vacancies link up to form the filament. Note that we are only interested in the first instance of forming here and not the subsequent growth of the filament. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

A good criterion to quantify the convexity is the ratio of the Weibull slope at the low and high percentile ranges (β_{LP}/β_{HP}). Fig. 3 plots the trend of β_{LP}/β_{HP} for three different oxide thickness values of t_{ox} = 2.4 nm, 3.2 nm and 4.0 nm. It is interesting to note that the convexity increases more for thicker dielectrics, possibly due to larger dominance of the GB column and the increasingly apparent difference in the ease of defect generation around the GB, as the number of defects needed to form the filament proportionally increase for thicker films.

To find out the number of filaments that nucleate at G and GB locations, Fig. 4 plots the histogram of the filament location distribution considering the length of the simulated dielectric region to be 250 cells (~8 Å × 250 = 200 nm). Three different λ_{GB}:λ_G ratios of (a) 1:1, (b) 2:1 and (c) 3:1 are considered here for t_{ox} = 4.0 nm. Since the first case is that of an amorphous film, we observe an almost uniform spatial distribution for filament nucleation in Fig. 4(a) (simulation consisted of 1000 trials for each scenario). As the λ_{GB}:λ_G ratio is increased, filaments tend to preferentially nucleate at the GB sites which are purposely placed at regular intervals in the simulation → one in every 30 columns corresponding to ~8 Å × 30 = 24 nm mean grain size, which matches closely with the grain size stochastics extracted previously from experimental STM studies on HfO_2 films [23]. The location of placement of GB is regularly patterned in our simulation only for simplicity. It is worth noting that a random or organized pattern of GB will yield the same results as we do not consider the interaction of defects from neighboring columns and nearby GB as a first order approximation.

In Fig. 5, we also show a box plot of the number of (a) G and (b) GB filaments for a wide range of λ for 250 simulation trials. The same qualitative result as in Fig. 4 is evident here. Moreover, we can conclude that if the λ ratio is one order of magnitude or higher, then almost all the filament nucleation events occur along the GB. The presence of GB therefore helps reduce the forming voltage (V_{FORM}) and power; though at the cost of this, we have to compromise with a large spread in the statistical distribution (Fig. 2(a)).

4. Impact of process induced defect distribution

The sputter deposition technique is one common method used for deposition of high-κ during fabrication of the MIM stack. Sputtering is a physically destructive process and it introduces a lot of random defects into the dielectric [24,25] as illustrated in Fig. 6(a). When the forming process is simulated on amorphous films to assess the separate impact of these process induced defects, we find an elongated shallow slope tailed distribution at low percentile values for higher average defectivity (p_{DEFECT}) as illustrated by Fig. 6(b). Therefore, while the sputter deposition process may assist in achieving forming-free RRAM by purposeful introduction of spatially random defects, it is detrimental in broadening the spread of the forming distribution quite significantly. With increasing defect concentration induced by sputtering for small area devices, the likelihood of nucleating large clusters of defects in some of the devices is high. This gives rise to the flattened distribution at low percentiles in Fig. 6(b). If we were to choose the atomic layer deposition (ALD) method, the damage caused would be much lower and we may not have to deal with this process induced extrinsic variability issue.

5. Metal–dielectric interface roughness issues

While the HfO_2 dielectric and silicon substrate had an atomically smooth interface for logic devices, the MIM stacks suffer from

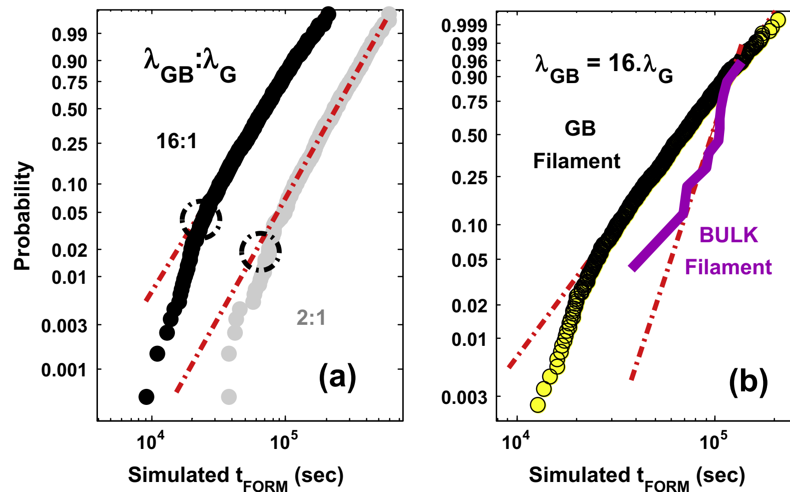

Fig. 2. (a) Weibull plot of the (a) forming time distribution assuming $V_{TE} = 2$ V for two different defect generation ratios of 1:2 and 1:16 for $t_{ox} = 3.2$ nm. (b) Plot of forming time at grain and GB sites extracted from the overall distribution in (a). The red dotted lines represent force-fitted Weibull distribution line to data. The deviation of data from the straight fit line at low percentiles is clearly evident. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

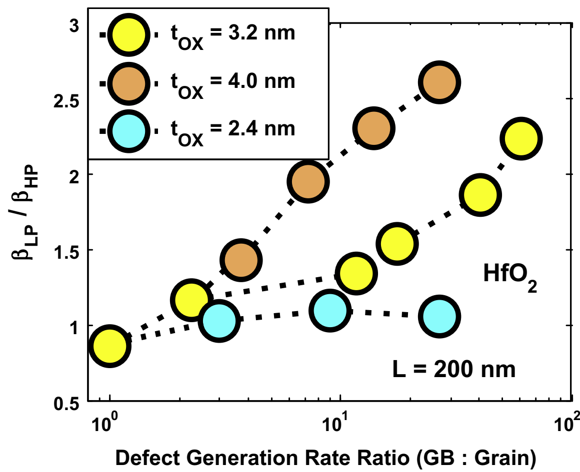

Fig. 3. Trend of β_{LP}/β_{HP} for three different dielectric thickness values. The convexity ($\beta_{LP}/\beta_{HP} \gg 1$) is more apparent for thicker dielectrics and increases with higher relative value of λ around the GB.

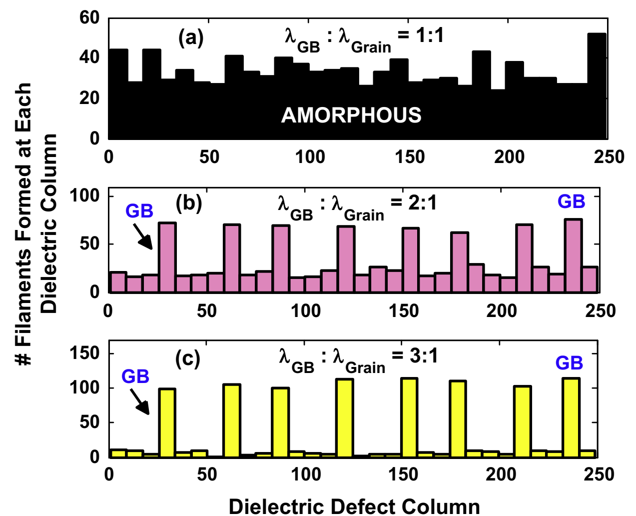

Fig. 4. Histogram plot of the number of nucleated films across different spatial locations in the simulated 2D dielectric film with 250 columns for three different vacancy defect generation rate ratios. The width of the grain is considered to be 30 columns wide.

rough metal–dielectric interfaces that can induce additional variability issues in the forming process because a rough dielectric translates to wide variations in the local dielectric thickness at different spots within the MIM capacitor. We considered three hypothetical scenarios for looking into the roughness effect. These were (a) atomically smooth interfaces at both top and bottom electrode, (b) rough interface at only one electrode interface with variation of one atomic layer ($\Delta t_{ox} = a_0$) and (c) rough interfaces at the top and bottom electrode sides with $\Delta t_{ox} = 2a_0$ (Fig. 7(a)). Note that we assume integral values of Δt_{ox} here for simplicity so that the percolation model could be utilized to simulate the change in the forming distribution trends. As shown in Fig. 7(b), while the forming distributions remain essentially Weibull, the spread increases quite significantly as the effective Weibull slope reduces for rougher interfaces. While the mean forming time had negligible dependence on the process induced random defect concentration (as evident in Fig. 6(b) of previous section), the roughness issue impacts the mean as well. In all the cases that we have been considering, the reduction in forming power (voltage) comes at the expense of increased variance in its distribution. These trade-offs are intrinsic to the device and have to be considered carefully when optimizing the design and operating conditions of the RRAM.

6. Impact of multi-layer high-κ films on forming

Since grain boundaries play a key role in the forming conditions and variance, we investigate the role of having two high-κ deposition steps with thickness each of $t_{ox}/2$, instead of depositing a single high-κ layer of t_{ox} in one step. The reason for considering this method is that the GB lines in the two-step processed films in each layer are likely to be misaligned with each other such that it becomes difficult to establish a connectivity path between the top and bottom electrodes (see inset of Fig. 8). This will enable lower power switching as the forming (soft breakdown) process occurs in stages. Such a proposal was made previously by Yew et al. [12] and experimentally shown to boost the lifetime of logic devices.

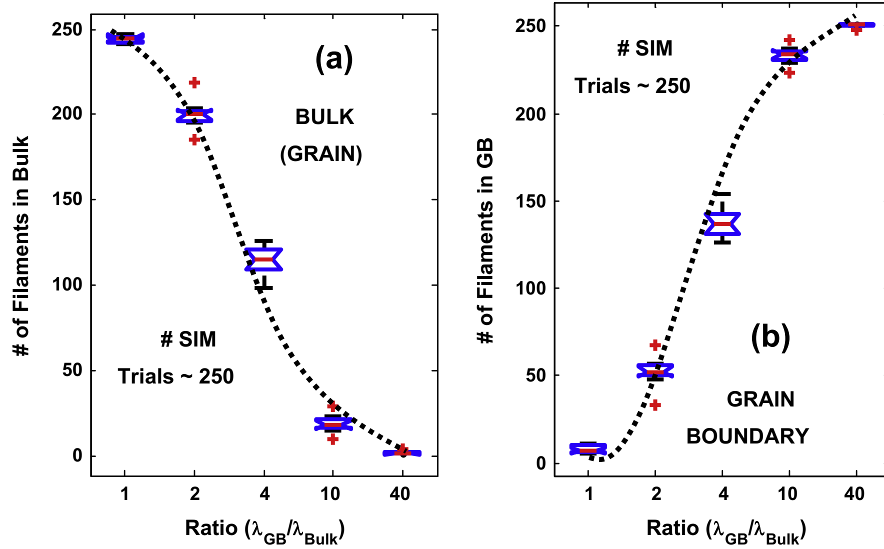

Fig. 5. Boxplot of the number of nucleated filaments at the (a) G and (b) GB sites for different ratios of defect (trap) generation rates.

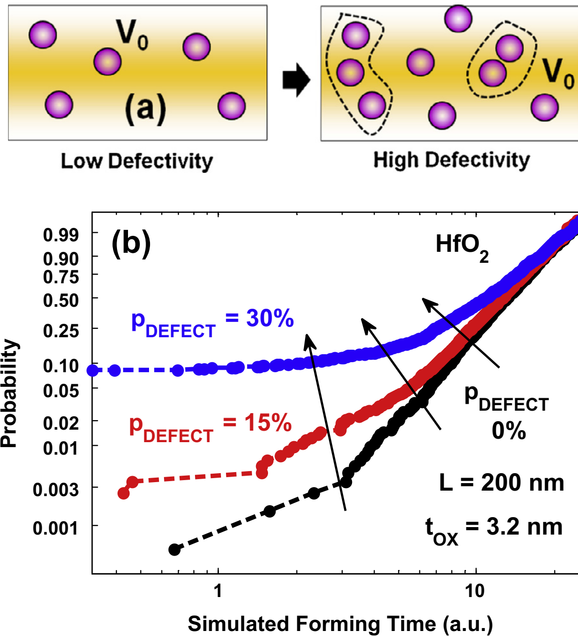

Fig. 6. (a) Illustration showing the process induced spatial defectivity in the dielectric where defects due to physical damage from sputtering process tend to nucleate. Some of these defects could form localized clusters as shown by the dotted borders. (b) Low percentile tailing and shallow Weibull slope observed as the number of sputter defects increases. Though sputtering may help reduce forming voltage, the resulting variance in forming parameters is far from acceptable.

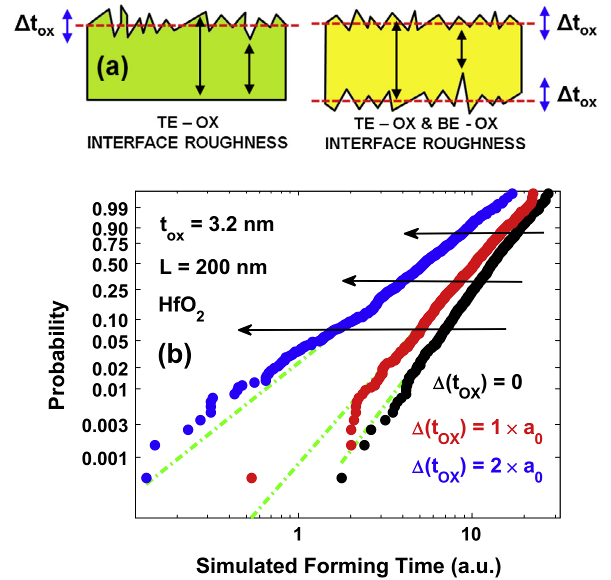

Fig. 7. (a) Illustration showing the atomically rough interface that could exist at the top and/or bottom electrode – dielectric interfaces. The bottom electrode interface is more prone to these roughness issues due to non-uniformity in metal electrode deposition. (b) Weibull plot of forming time comparing atomically smooth interface with rough interfaces at one electrode end and both ends.

In the context of RRAM, the impact of having a dual-layer dielectric stack on the forming distribution is worth investigating. Previous reports have shown that the existence of dual layer stacks may ensure better control in the shape and size of the filament that is formed [26]. However, deciphering the distribution of t_{FORM} or V_{FORM} is non-trivial considering the electric field distribution which depends on the number of aligned and non-aligned GB columns as well as the change in field distribution once one of the dielectric suffers a SBD.

The simulated forming time distribution comparing single versus two stage high-κ deposition for t_{ox} = 4.8 nm is shown in Fig. 8, where we modeled the GB in the two layers to be purposely misaligned with each other, which is the most practical scenario. After the filament has first formed in one of the layers, the κ value is assumed to increase to 28 for the oxygen depleted region where the filament nucleated (analogous to dielectric soft breakdown and percolation path creation). The voltage drop across the two layers is re-calculated using the Gauss law before and after the filament nucleates in one of the layers. It is worth noting that when there are two high-κ films with a region where one layer has a GB and the other layer has a grain, the Gauss law and defect generation rate calculations show that the rate is higher in the grain region than in the GB in the other film. This is because the GB is intrinsically a low resistance region and a majority of voltage therefore drops across the other layer (G). In short, GB directs the filament to be nucleated in the bulk grain region beneath or above it.

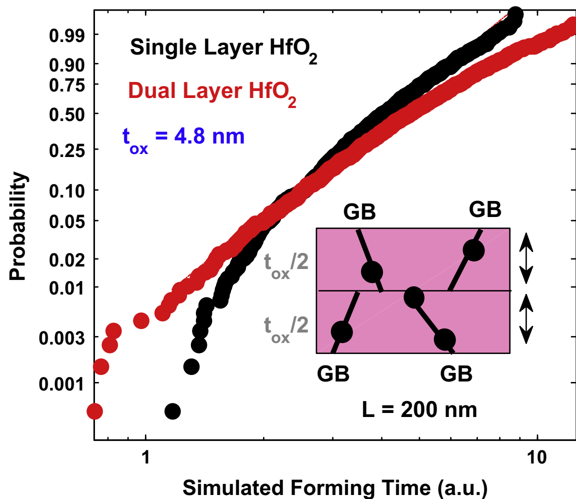

Fig. 8. Comparison of the forming time distribution for a single stage and dual stage deposition of HfO_2 high-κ film (with same overall thickness of $t_{ox} \sim 4.8$ nm). The key difference between these two deposition schemes is the misalignment introduced in the GB lines for the two films. The black circles in the inset illustration represent pre-existing vacancy defects at the GB site.

From Fig. 8, while the mean forming parameters have not changed much with the two-stage deposition process flow, the tail gets longer and Weibull slope (β) is shallower for the dual layer stack. This could be attributed to the fact that the first forming event is now governed by a thinner dielectric (half of the original thickness). Since dielectric breakdown studies show a clear linear dependence of β on t_{ox} [27], the wider spread in the forming time distribution is an expected outcome.

Although this decrease in β is actually not desirable, the advantage of having a dual layer stack is that a majority of the simulation trials end up with filament locations in the two dielectric layers being uncorrelated to each other as shown by the scatter plot in Fig. 9. As a result, we may use this two-stage deposition technique to successfully demonstrate ultra-low power (low current) switching devices because there is no direct full defect connectivity path (short) between the top and bottom electrodes even after the full filament is formed, which in turn translates to low power operation ("very soft" forming). In Fig. 9, we consider two different κ values for the GB. As the κ_{GB} value increases, the number of (GB + grain) filament increases, while the count for purely bulk region filaments is lower. Note that the dot pattern is more organized and patterned in Fig. 9(a) for $\kappa_{GB} = 26$, as 45% of the filaments nucleated at the GB sites which we placed at regular intervals along the simulated percolation cell framework. However, with lower κ_{GB}, the dot pattern is more randomized (Fig. 9(b)) since only 10.8% of the filaments nucleated at the GB site, when 1 in every 30 (3.33%) columns corresponded to the GB.

Another fact to consider is that thinner dielectrics have a much higher crystallization temperature. As a result, while a 4.8 nm single layer high-κ film may have a lot of GB, the probability of reaching a polycrystalline state is drastically reduced for 2.4 nm films. Therefore, there is a likelihood of having an amorphous stack with the filament locations being all the more uncorrelated (implying larger proportion of devices with "very soft" forming).

7. Conclusions of study

Various non-ideal process and material factors that affect the variability in the forming conditions were explored in this study by means of a 2D percolation cell framework to model oxygen vacancy thermochemical defect generation in HfO_x-based RRAM. The adverse effects of deposition process induced extrinsic defect distribution and the interface roughness issue on the increasing spread of forming time was clearly evident. While the presence of GB helps reduce forming power, it also broadens the variability component. The use of dual layer high-κ films was explored and though it adversely impacts the variability trends, the positive feature is that uncorrelated filament spots in many devices could help achieve very 'soft forming' and ultra-low power non-volatile memory device operation. Further experimental initiative is needed to verify the above stochastic simulation results and the study can potentially be used to tune the process and material stack of RRAM so as to tighten the spread in the forming process and lower the forming voltage/power at the same time.

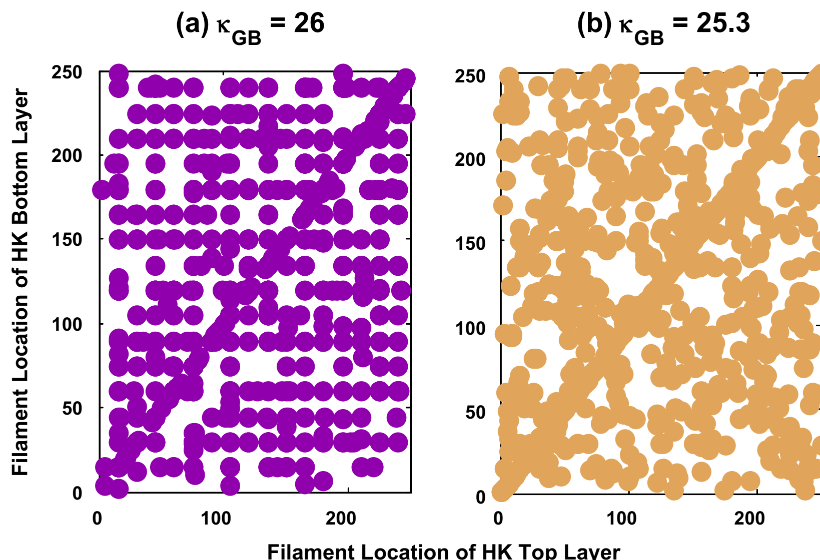

Fig. 9. Correlation of the filament location in the top and bottom layer of the two-stage deposited high-κ film for (a) $\kappa_{GB} = 26$ and (b) $\kappa_{GB} = 25.3$. The number of correlated nucleation events (points that fall on the $y = x$ line) increases with κ_{GB}; however a majority of the filament spots are still uncorrelated due to the GB misalignment. To simulate the misalignment, we placed the GB columns in the two films offset by half the grain size.

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