Spectroscopy of SILC Trap Locations and Spatial Correlation Study of Percolation Path in the High-κ and Interfacial Layer

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Abstract — **It has always been assumed all along that the percolation path in the high-κ (HK) and interfacial layer (IL) of dual layer dielectric stacks are perfectly aligned with each other. There is however no solid evidence to date to support this assumption because the standard stress levels applied and compliance chosen for time dependent dielectric breakdown (TDDB) tests is high enough to instantaneously rupture both the HK and IL layers, once one of them reaches the percolation stage of degradation. The aim of this study is to probe the location of the HK and IL percolation paths and study their correlation by means of a novel TDDB test algorithm that enables a finite time two-stage event of BD for the dual layer stack with only one dielectric percolating during each stage of stress. The analysis reveals that although in most cases the HK and IL layers have the BD location very close to each other, there are cases of slight misalignment that can be advantageous from a reliability viewpoint as misaligned percolation paths result in a much lower leakage current (even in the logarithmic scale) as compared to the perfectly aligned ones. We also extend this analysis to probing the locations of different stress induced leakage current (SILC) defect clusters in the dielectric prior to any breakdown event.**

Keywords – Breakdown location; Defect cluster; Percolation; SILC; TDDB.

I. INTRODUCTION

In-depth study of various failure mechanisms inherent in high-κ (HK) – interfacial layer (IL) dielectric stacks have been carried out over the past decade [**1**] – [**4**], considering that it is a functional unit of the transistor and memory devices used today in all digital electronic circuits and modules. Of the various degradation phenomena that HK dielectrics can exhibit either due to their own vulnerability or due to the imperfect interfaces they have with the surrounding materials in the device, time dependent dielectric breakdown (TDDB) is a critical one. It is well established that the random defect generation (if the dielectric is amorphous) in the oxide results in percolation path formation which is termed “TDDB” [**5**, **6**]. The TDDB and post-breakdown (BD) kinetics have been extensively investigated from electrical [**7**], physical [**8**] and statistical viewpoints [**9**] – [**11**] and several compact models [**12**] and first-principle [**13**] and Monte Carlo simulations [**4**, **14**] have been carried out to better understand the material structure and operational conditions that favor the kinetics of these failure mechanisms. In spite of the vast knowledge gained in this field, one critical consideration that has not been fully thought of is whether the breakdown location (percolation path) for the HK and IL are correlated and aligned with each other. This is an issue only in dual layer stacks as there is just a single percolation event in the case of SiON / SiO_2 for older CMOS technology nodes. Currently, it is always assumed that the percolation paths in the HK and IL are perfectly aligned with each other. While this is logical and reasonable to assume, this study aims to develop a TDDB test methodology to break down the HK and IL layers in two distinct stress steps and apply it to extract the percolation locations in the HK and IL separately, so that the validity of the assumption can be examined.

The problem with current TDDB test approaches in the industry is that the stress level is too high (especially in small area devices) and the compliance levels are arbitrarily chosen to be as high as 50-100μA [**15**, **16**], as this was the traditional practice adopted for SiON / SiO_2. In the case of HK-IL stack, when the first layer breaks down, there is a significant re-distribution in the voltage levels such that the second layer experiences a higher field that could cause it to percolate immediately as the magnitude of this field could be closer to or even higher than the critical field strength (ξ_{CRIT}) of that material. This is the reason why HK-IL stacks show a single stage abrupt BD when stressed at highly accelerated conditions.

Our analysis here involves a multi-stage ramped voltage (*I-V*) TDDB stress algorithm (slow ramp rate) with successively higher compliance levels of I_{comp} ~ 0.1μA, 0.4μA and 5μA. All the tests were carried out on small area NMOS devices (W × L = 0.5 × 0.25μm^2) at T = 298K with t_{HK} = 44Å and t_{IL} = 8Å representing the thickness of the two dielectric layers (as confirmed previously by physical microscopy analysis [**17**]). The high-κ material here is polycrystalline HfO_2 and the gate electrode is specifically chosen to be polysilicon for reasons that will be discussed later. The three different I_{comp} values have been carefully chosen to arrest the device at the SILC stage, after one-layer BD and after two-layer BD.

The structure of this work is organized as follows. In Section II, we shall explain the alternating stress and sense test methodology developed for creating defect clusters and nucleating percolation paths in the HK and IL. The analysis of the SILC defect cluster locations will be presented in Section

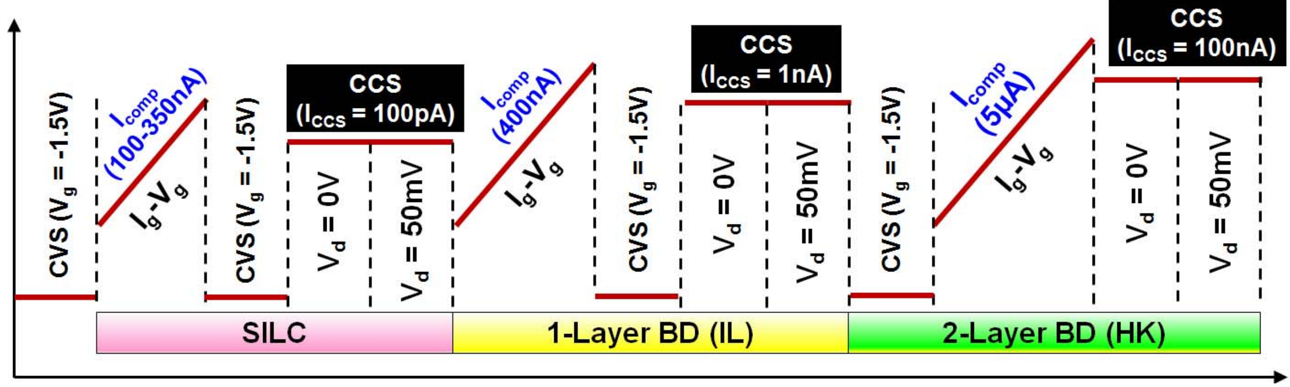

Figure 1. Different stages and sequence of the *I-V* procedure for inducing SILC defect cluster generation, one-layer BD and then two-layer BD. At each stage, after the stress, multiple sensing signals are applied that include constant voltage stress (CVS) at -1.5V (NMOS transistor in accumulation) as well as constant current stress (CCS) to measure the gate voltage drop at two different drain conditions of V_d = 0V and 50mV, so that the defect / percolation locations could be mapped.

III, followed by the estimation of the first percolation location in Section IV using a simple theoretical derivation to estimate the location of the BD spot. In Section V, the location of the second BD spot is estimated and its correlation with the first BD spot in the other layer is studied both from our electrical test results as well as Monte Carlo simulation studies. Finally, the new understanding gained from this study is summarized in Section VI and the study concludes with implications of the findings and the justification for the specific use of polysilicon based gate electrode.

Although the methodology proposed this study is insensitive to whether the HK or IL break down first, the following sections will consider IL to be the weakest link which percolates first, followed later by the HK. Our evidence of IL-induced failures are based on accelerated TDDB stress tests on HK-IL stacks in which the activation energy for the bond breaking process (E_{a-BB}) based on the thermochemical model, extracted from the time to failure data match very closely with the E_{a-BB} value for conventional SiO_2 / SiON [**18**]. Moreover, using Kinetic Monte Carlo (KMC) studies as well [**19**], the IL seems to be the first to fail based on the voltage distribution across the two layers, taking into account the lower thickness and higher permittivity (κ_{IL} ~ 6 >> κ_{SiO2} ~ 3.9) in the oxygen-deficient sub-stoichiometric IL layer (SiO_x, x << 2) which causes the electric field in the IL (and hence the defect generation rate) to be much higher than in the HK. Several recent results have also claimed IL to be weakest link in the dual layer gate stack [**9**, **20**-**24**].

II. Proposed Test Methodology

The multiple stress and sense signals applied to the NMOS device and their sequence is shown in Fig. 1. Each of these signals are purposely applied so as to extract some information on the location of the percolation paths. The constant voltage stress (CVS) signal of V_g = -1.5V is used to measure the proportion of the source (I_s) and drain currents (I_d) and their directions (flowing into / out of the gate). The simplest formula that is generally used for BD location estimation in the accumulation mode is $s_{BD} = I_d / (I_d+I_s)$ [**25**]. However, this is only applicable when the complete stack has broken down. We will derive a different formula here for estimating s_{BD-IL}, while the above formula can be used as per normal for s_{BD-HK} (HK+IL BD). We measure the CVS data at V_g = -1.5V for the initial unstressed device as well because the estimation of s_{BD} for each stage is not based on the absolute values of I_d and I_s; rather it is based on the relative change ΔI_d and ΔI_s for each successive stage of degradation / breakdown. For example, if we intend to calculate the location of the predominant defect cluster after SILC stress (s_{SILC}), we should calculate the values of ΔI_d and ΔI_s relative to the fresh device. Similarly, to calculate the value of s_{BD-IL}, the expression should be $\Delta I_d = I_{d-IL-BD} - I_{d-SILC}$ and $\Delta I_s = I_{s-IL-BD} - I_{s-SILC}$ and so on.

The constant current stress (CCS) signal is measured at two different drain voltages with ΔV_d = 50mV, as the difference in the gate voltage levels for the two different V_d values can be used to compute the location of a defect in the dielectric, as recently reported by E. Bury *et al.* [**26**]. The CCS values of 100pA, 1nA and 100nA (indicated in the black shaded boxes in Fig. 1) for CCS are chosen such that the defects respond frequently and repeatedly at the different stages of degradation with relatively moderate voltage drops across the dielectric (without stressing it any further).

III. Spectroscopy of SILC Defects

When the I_g-V_g ramp stress is halted at I_{comp} ~ 0.10-0.35µA (exact I_{comp} depends on initial leakage levels / process induced defects in the device), we may use the I_g-V_g sweep at V_d = 0V and 50mV (ensuring that the transistor is in the linear regime) to estimate the location of a trap / defect using Eqn. (1), where $L_{channel}$ is the length of the transistor channel and X_{trap} is the location of the trap. This formulation was used for detecting the location of a single trap-assisted tunneling (TAT) defect in the SiON based MOS device by E. Bury *et al.* [**26**] recently. Here, we extend this approach by using a CCS scheme instead of an I_g-V_g sweep so that the location of multiple defects in the SILC stage which would respond in the form of a random telegraph noise (RTN) could be mapped using the same formula in Eqn. (1). In other words, the different discrete ΔV_g values that we would obtain by comparing the V_g RTN signals at V_d = 0V and 50mV will enable us to map all the active defects in the SILC stage. If however, the interest is to find the predominant largest defect cluster, this information would be reflected by the estimated value of s_{SILC} calculated using ΔI_d and ΔI_s. As an example, one of the RTN signatures observed is shown in

Fig. 2 with I_{CCS} set to 0.35µA. Clearly, 3-4 different levels of V_g are observed which could correspond to at least two active defects in the oxide. Using this method repeatedly on several devices, we present in Fig. 3 a dot map of the SILC defects for 7 similar devices. It is to be noted that this technique only gives us the locations of the different SILC defects, but not the cluster size of these defects. As mentioned earlier, an estimate for the largest cluster defect could be obtained by calculating s_{SILC} using the standard formula (derived in Eqn. (5) later). The analysis on s_{SILC} will be presented together with $s_{BD\text{-}IL}$ and $s_{BD\text{-}HK}$ in the later section. From Fig. 3, it is clear that the defect generation in the SILC stage is "fully random" and not confined to the corners in particular.

$$X_{trap} = L_{channel} \cdot \left(\frac{\Delta V_g}{V_d} \right) \tag{1}$$

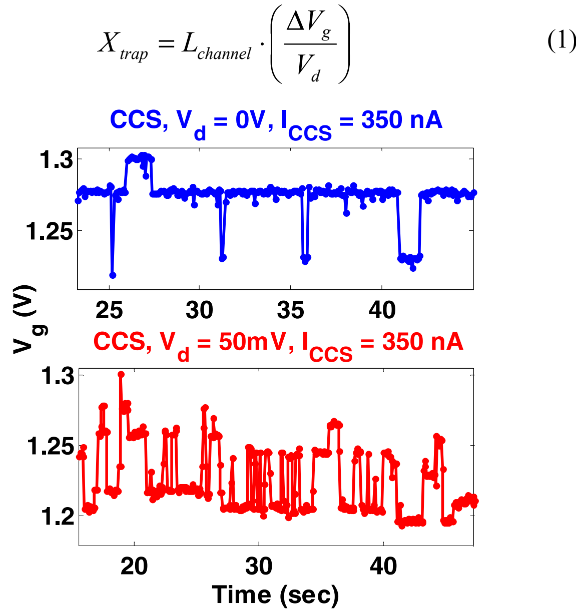

Figure 2. Random telegraph noise (RTN) signatures at V_d = 0V and 50mV for one of the devices stressed to the SILC stage. The CCS here is carried out for a moderate period of time to maximize the chances of detecting as many defects as possible (both the slow and fast traps).

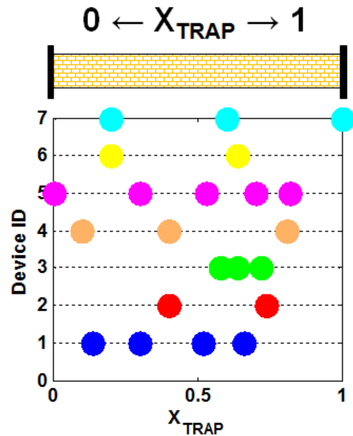

Figure 3. Dot map of the *x*-direction defect locations (X_{trap}) for 7 similar devices tested using the same methodology shown in Fig. 1.

IV. Estimation of First Layer Breakdown Location

As mentioned earlier, there is sufficient evidence in support of our claim that the IL is the first layer to break down during the TDDB stress [**9**, **18-24**]. In order to detect the breakdown location, the standard formula given by Eqn. (2) (which will be used later to calculate $s_{BD\text{-}HK}$ after full percolation of bi-layer stack) cannot be directly applied because the derivation of that expression is based on the assumption that both I_d and I_s currents flow head on towards each other and enter into the gate terminal together (Figs. 4(c, d)). Such a scenario is plausible only for a hard breakdown (HBD) event when both the dielectrics are substantially damaged and the percolation resistance (R_{perc}) becomes comparable to the channel resistance (R_{ch}). However, our observations in soft breakdown (SBD) mode (R_{perc} >> R_{ch}) after one-layer BD show that the I_d and I_s currents are generally opposite in direction to each other (Figs. 4(a, b)) and hence a fundamental simple derivation for estimation of $s_{BD\text{-}IL}$ is required, as shown by Eqns. (3)-(5), accounting for the relative change in ΔI_d and ΔI_s, instead of the absolute values of I_d and I_s.

$$s_{HBD} = s_{BD-HK} = \frac{\Delta I_d}{\Delta I_d + \Delta I_s} \tag{2}$$

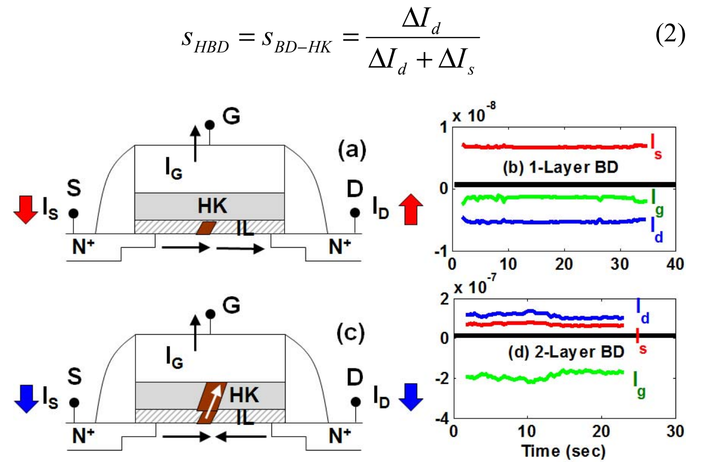

Figure 4. (a, c) Schematic showing the directions of I_d and I_s in the transistor after one-layer and two-layer BD respectively. (b, d) Experimental data showing that the I_d and I_s currents have opposite signs for one-layer BD, while they flow in the same pattern (same sign) into the channel for two-layer BD.

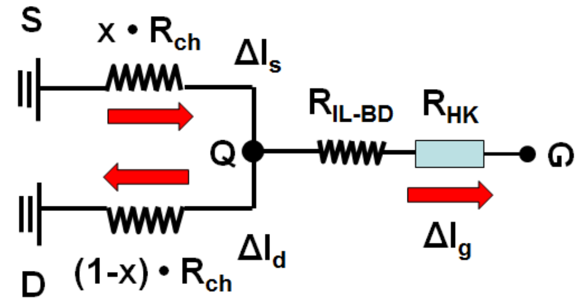

Figure 5. Circuit diagram showing the resistances in the channel and the dielectric after one-layer (IL) BD. The corresponding lumped resistors are labelled accordingly. Here, R_{HK} >> {$R_{IL\text{-}BD}$, R_{ch}}, as the HK layer is still intact and the Δ symbol is added to the current flow to denote the relative increase in their values before and after the one-layer BD.

The simple resistive circuit diagram for IL-only BD is shown in Fig. 5, denoting Q as the point along the transistor channel, where the percolation has occurred. The Ohm's law expressions for V_{SQ} and V_{DQ} are given by Eqns. (3) and (4) where x is the relative location for the percolation spot and $x=0$ and $x=1$ represent the source and drain terminals respectively.

Imposing the condition $V_{SQ} = V_{DQ}$, the final expression for x is given by Eqn. (5). This is the formula to be used for computing the value of $s_{BD\text{-}IL}$ in this study. Note the change in sign for the denominator in this expression, when compared to the standard one in Eqn. (2). It is the change in directions of I_s and I_d flow that brings about this change in sign.

$$V_{SQ} = 0 - \Delta I_s \cdot (x \cdot R_{ch}) \tag{3}$$

$$V_{DQ} = 0 - (-\Delta I_d) \cdot ((1-x) \cdot R_{ch}) \tag{4}$$

$$\begin{aligned} & V_{SQ} = V_{DQ} \\ \Rightarrow & -\Delta I_s \cdot (x \cdot R_{ch}) = \Delta I_d \cdot ((1-x) \cdot R_{ch}) \\ \Rightarrow & \quad x \cdot (\Delta I_d - \Delta I_s) = \Delta I_d \\ \Rightarrow & \quad x = s_{BD-IL} = \left(\frac{\Delta I_d}{\Delta I_d - \Delta I_s} \right) \end{aligned} \tag{5}$$

It is necessary to question the validity of our claim that the currents I_s and I_d flow in opposite directions after one-layer BD. While most of the tests show opposite polarity signs for these two currents after one-layer BD, some cases with like polarity are also observed. Our speculation here is that the right polarity for I_s and I_d is decided by the "breakdown hardness" which in turn depends on how effectively the external compliance setting controls the "percolation transient" within the IL layer. Since these transients are ultra-fast events that only need time in the nanoseconds range [**27**], the compliance control may sometimes not be as effective and may cause the subsequent HK layer to wear-out and/or partially percolate. This variation in breakdown hardness explains the fluctuating polarity values in I_s and I_d for different tested devices. Our method here is highly sensitive to the manual setting of I_{comp} as the difference (gap) between the user-set value of I_{comp} and the current level at which the percolation transient begins determines the probability of uncontrolled breakdown. It is to be noted though that further analysis only considers cases of well controlled percolation wherein I_s and I_d are of opposite polarity as illustrated in Fig. 4(a, b) when the condition $R_{perc} >> R_{ch}$ is satisfied.

V. Percolation Location Correlation in HK and IL

Having established the method for calculating the percolation location ($s_{BD\text{-}IL}$) after one-layer (IL) BD in the previous section and knowing that the calculation of $s_{BD\text{-}HK}$ is a straightforward one based on Eqn. (2), we may now assess the spatial correlation between these two values, which was the main motive of our study.

A. *Correlation in the HK and IL Percolation Locations*

The normal probability plot of s_{SILC}, $s_{BD\text{-}IL}$ and $s_{BD\text{-}HK}$ extracted from our electrical tests on 15-20 devices is plotted in Fig. 6. Note that the predominant SILC cluster location in different devices is quite randomly distributed (Fig. 6(a)). However, although there is considerable spread in $s_{BD\text{-}IL}$, a large fraction of the devices ended up having the IL percolation close to the center of the channel (Fig. 6(b)), which is in good agreement with the analysis on pure SiON devices in Ref. [**26**]. Analyzing the spread in $s_{BD\text{-}HK}$, most of the percolation spots are localized at $s = 0.5$ (Fig. 6(c)). When these results are plotted as a scatter plot of s_{SILC} versus $s_{BD\text{-}IL}$ (Fig. 7(a)) and $s_{BD\text{-}IL}$ versus $s_{BD\text{-}HK}$ (Fig. 7(b)), we do not observe significant correlation between the SILC and IL BD spots. This means that the most predominant SILC cluster does not necessarily have to be the location of the first IL BD event. There is still a finitely large probability that the IL could percolate elsewhere unrelated to the largest SILC defect cluster.

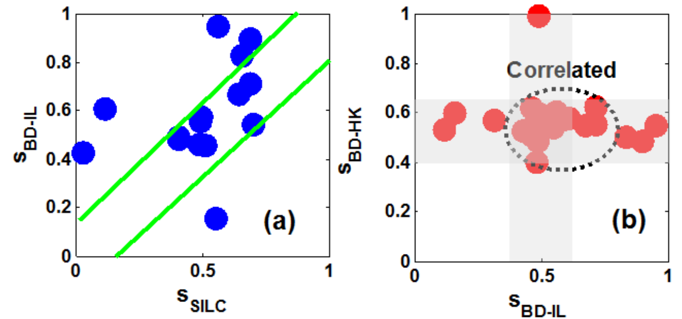

Figure 6. Scatter plot of (a) s_{SILC} with $s_{BD\text{-}IL}$ when the device stress is arrested at $I_{comp} \sim 0.4\mu A$ and (b) $s_{BD\text{-}IL}$ with $s_{BD\text{-}HK}$ after the stress is continued and I_{comp} set to $5\mu A$.

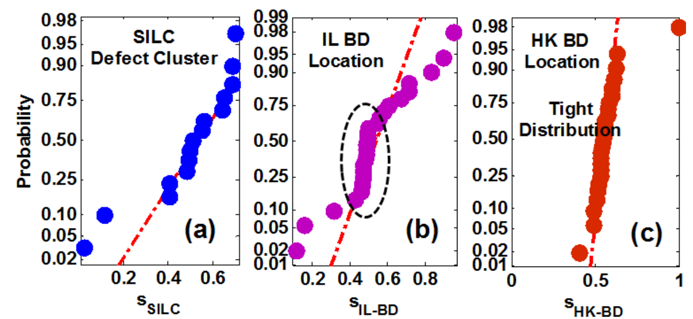

Figure 7. Normal probability plot of (a) s_{SILC}, (b) $s_{BD\text{-}IL}$ and (c) $s_{BD\text{-}HK}$ from the measured device test results.

The situation is different when comparing $s_{BD\text{-}IL}$ with $s_{BD\text{-}HK}$ in Fig. 7(b). A large proportion of the devices (73% of them) seem to have the percolation paths in the HK and IL very close to each other (with some slight misalignment) and at the center of the channel. This confirms the general assumption that the HK and IL BD paths are in line with each other. It is critical however to note that about one-fourth of the devices tested have a large difference between $s_{BD\text{-}IL}$ and $s_{BD\text{-}HK}$.

From a reliability point of view, if the HK and IL percolation paths are even slightly misaligned from each other, the defects do not perfectly connect the gate and substrate which causes the leakage current to be substantially lower. This is good news because it implies that some devices may not affect circuit performance (power dissipation) much even if the complete stack were to break down. The take away message from the analysis here is that not all break down events are perfectly correlated. In a circuit with a billion transistors, this stochastic spread in percolation path misalignment will in turn contribute to additional variability in the circuit parameters. With HK dielectrics tending to be polycrystalline with grain boundary (GB) fault lines randomly spread across the thin film and given that these GBs serve as

preferential locations for breakdown [**28**], the likelihood of IL and HK percolation misalignment should not be surprising given that IL is amorphous and HK is polycrystalline in microstructure.

B. Monte Carlo Analysis of Percolation Misalignment

To further confirm the findings from our electrical test results, a Kinetic Monte Carlo simulation of the defect generation process was carried out for the HK-IL stack accounting for the local re-distribution of voltage after one-layer BD (above or below the percolation spot) according to the Gauss Law with 500 simulation trials each time for a given set of dielectric thickness values. For details on how the simulation is carried out, readers may want to access Ref [**14**]. The percolated region in the IL after one-layer BD is modeled with different local permittivity (κ_{IL-BD}) values ranging from 6 to 7, where κ_{IL-BD} increases with higher oxygen vacancy density. The "softer" the BD, the lower is the value of κ_{IL-BD}.

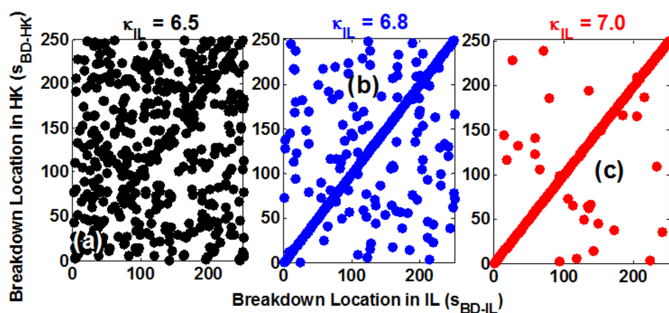

Figure 8. Monte Carlo simulation based estimation of s_{BD-IL} and s_{BD-HK} for three different permittivity values of the IL layer percolation spot (representing different densities of vacancy defects) ranging from $\kappa_{IL-BD}\sim$ 6-7.

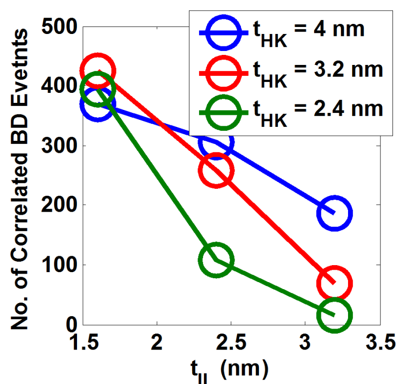

Figure 9. Plot of the number of correlated IL and HK BD events for different thickness combinations of the IL and HK layers. For each thickness ratio (t_{IL} : t_{HK}), 500 Monte Carlo simulation trials were carried out.

Based on the results of the simulation run which detects the locations of percolation, a scatter plot of s_{BD-IL} and s_{BD-HK} is shown in Fig. 8 which reveals that anywhere between 3-74% of the devices could have correlated IL and HK percolation paths (large variation) and this correlation is a strong function of the "softness" of IL BD, i.e. the value of κ_{IL-BD}. Any misalignment in the IL and HK percolation paths could be explained by the fact that the IL-BD is "so soft", that the increment in electric field in HK layer directly above may not be sufficient enough to compensate for the area scaling effect of the bulk HK region failure. This idea is more clearly illustrated in Fig. 10 later).

Moreover, the extent of correlation also depends on the dielectric thickness combination of the HK and IL layers (t_{HK}: t_{IL}). As plotted in Fig. 9 which shows the mean number of correlated BD events for different values of t_{HK}: t_{IL}, there is a greater alignment of the percolation events when the HK is thicker and IL is thinner.

C. Summary of the Different Percolation Scenarios

The different possible scenarios for the percolation path locations in the HK and IL are illustrated in Fig. 10. *Scenario I* is where there is a partial alignment in the percolated locations which is widely prevalent in our electrical test results. The extent of misalignment determines how leaky the device is going to be after the two-layer BD. *Scenario II* corresponds to the case of a perfect alignment in the percolation path which causes the breakdown process to induce more damage, as a result of which, we may expect the lateral size of the BD spot to be much larger (as the wider black shaded regions represent). And lastly, *Scenario III* is one with no correlation at all, i.e. the HK and IL percolate at totally different locations. Such events, although rare (cannot be ruled out), are finite in number both in our experiments and simulation results.

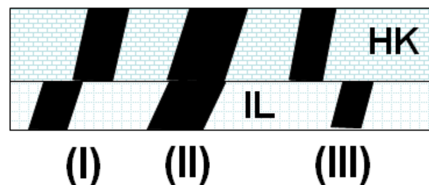

Figure 10. Illustration showing the three different plausible scenarios for percolation location correlation in the HK and IL layers with the size of the percolated region depending on the extent of misalignment in the defect path of the two dielectrics. Here, the width of the percolation path increases in the order → *III* < *I* < *II*.

VI. CONCLUSION

This is the first such study that presents a simple methodology enabling us to decouple the location of the BD path in the HK and IL layer. The crux of the approach lies in being able to carefully arrest the BD of each dielectric by precisely choosing the compliance values during the SILC-TDDB stage. Electrical test results indeed confirm the standard assumption that HK and IL BD events are largely correlated, but also point to the "finite" possibility of a small fraction of devices with different degrees of percolation path misalignment. If the percolated regions are misaligned, the leakage current could be significantly lower even after complete BD of the whole stack as the defect clusters are not fully connected requiring some tunneling event (not just thermal hopping) for electron conduction implying lower power dissipation. However, the different degrees of misalignment induce an additional source of variability in the circuit performance parameters.

It is worth noting that the scenario of (IL + HK) BD presented here is markedly different from the multiple BD scenario that has been investigated in the past [**29**, **30**]. In the

case of multiple BD, we consider the probability of nucleation of more than one full percolation path (and its spatial correlation) across the dielectric stack in a large area device / circuit. Here, our analysis is confined to focusing on just the very first full percolation event which in itself is a two-stage sequential BD process (with finite likelihood of misaligned "mini" percolation paths) for a two-layer oxide stack. In our previous studies [**19**], we have already proven both using electrical studies and thermochemical simulations that at the circuit level, for an operating voltage, V_{op} = 1V, circuit failure is most likely to occur only due to multiple soft BD events "within" the IL layer, while the HK film stays robust and intact (without percolating). It is only at the device level under relatively higher stress levels (relevant for accelerated reliability tests) ($V_{stress} > V_{op}$; $V_{stress} < V_{BD}$) that the HK and IL may both break down in the manner illustrated in Fig. 10. This in turn implies that extrapolating the HK-IL BD results from accelerated stress tests to operating conditions is much more challenging and non-trivial than one could expect.

Critical to mention, a study like this can only be carried out on poly-silicon electrode based devices and not on silicide and metal gates. This is because when the device is sensed in accumulation mode for estimating s_{BD}, the oxygen ions (liberated from oxygen vacancy defects (Si-O or Hf-O) and stored in the oxygen soluble metal electrode during the inversion stress phase) could drift back and passivate the defects (resistive switching effect) causing the percolation path to partially shut-off in the case of silicide and metal gates. Since poly-silicon is not oxygen soluble [**31**], the oxygen ions tend to react with it and do not drift back when the NMOS device is probed in accumulation. While we have assessed the BD location only along the length of the transistor channel, we are unable to probe these location details in the width direction. This requires the use of more specialized test structures [**32**], which could be a topic worth of further investigation.

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