Understanding Defect Kinetics in Ultra-Thin Dielectric Logic and Memory Devices using Random Telegraph Noise Analysis

N. Raghavan[1], W.H. Liu[2], R. Thamankar[1], M. Bosman[3] and K.L. Pey[1,♣]

[1]*Engineering Product Development (EPD) Pillar, Singapore University of Technology and Design (SUTD), Singapore – 487 372.*

[2]*Division of Microelectronics, School of EEE, Nanyang Technological University (NTU), Singapore – 639 798.*

[3]*Institute of Materials Research and Engineering (IMRE), A*STAR, Singapore – 117 602.*

♣Ph: (+65) 6303 6617, E-mail: peykinleong@sutd.edu.sg

Abstract — **The root cause of degradation and failure in nanoscale logic and memory devices originates from discrete defects (traps) that are created in the ultra-thin dielectrics during fabrication (process-induced) and / or voltage and temperature stress (stress-induced). In order to probe the chemistry of every discrete trap in terms of its bond state, charge state, physical location, region of influence, activation (relaxation) energy and trap depth below conduction band, low frequency noise (LFN) based measurement and analysis is a good approach as the random telegraph noise (RTN) signals which form the characteristic behavior of every trap undergoing stochastic carrier capture and emission process contain a wealth of information on the defect energetics. With nanodevices still undergoing aggressive device scaling, the presence of a finite number of discrete defects in logic and memory devices makes it easier to collect RTN signals and analyze them in detail. This study presents an overall perspective to current developments in RTN-based studies on logic and memory devices and their impact on the variability in performance metrics. This is by no means an exhaustive overview; however, the key advancements in RTN as an effective defect spectroscopy tool are highlighted.**

Keywords –Breakdown; Defect (Trap); Filament; Random telegraph noise; Read disturb.

I. INTRODUCTION

Noise is an important signal to be analyzed in the design, test and qualification of nanodevices. On one hand, it provides a lot of scientific insight into the nature of the defect (trap) including its geometric position, bond configuration, charge state (Si^{1+}, Si^{2+} etc.), trap depth and activation energy. On the other hand, its magnitude, frequency and Poissonian nature have an adverse impact on the variability of the performance parameters (such as drain current, I_d, threshold voltage, V_{TH}) and lifetime with respect to different front-end failure mechanisms (time dependent dielectric breakdown → TDDB, bias temperature instability → BTI). Measuring noise in the low frequency (typically in the range of 10-100 Hz) during different stages of degradation and breakdown of the nanodevice helps in assessing the change in defect density and the different trap behavior with time / stress / local temperature etc. With this in mind, the study here presents the latest developments in RTN based analysis of logic and memory devices and the scope for further investigation in this field of work. For illustrative purposes, some results on planar high-κ transistors, blanket high-κ films and resistive random access memory (RRAM) devices will be presented.

The outline of this paper is as follows. Section II talks about the correlation between the gate (I_g) and drain current (I_d) in NMOS devices and how they are correlated / uncorrelated to each other. In Section III, the impact of RTN noise on BTI shift and the relation between BTI and RTN is summarized based on the recent work from other research groups. This is followed by a discussion of the impact of RTN on the memory window in RRAM and the non-steady state noise at low voltage read conditions in the high resistance state (HRS) due to read disturb issues. Section V presents a novel approach of being able to characterize individual defects using a scanning tunneling microscopy (STM) tool on blanket oxide films with high spatial and temporal resolution. Finally, we conclude the study with a summary identifying potential areas for further scientific research on noise based diagnostics and prognostics.

II. GATE AND DRAIN CURRENT CORRELATION

There are several studies [**1**] – [**3**] that report correlated and uncorrelated patterns of RTN when I_g and I_d are simultaneously measured. The presence or absence of correlation provides some insight to the physical location of the defect from the Si-dielectric interface in MOS transistors. Defects that are located far away from the Si-SiO_x interface are likely to impact only the gate current, while defects closer to the interface may tend to interact more with the discrete dopants in the transistor channel causing I_d fluctuations. Note that most high-κ stacks consist of a sub-stoichiometric SiO_x layer sandwiched between the high- κ and Si, referred to as interfacial layer (IL).

Fig. 1 shows the measured I_g - I_d trend in an NMOS device at T = 150K after soft breakdown (SBD) with V_g = {0.6, 0.7}V and V_d = 50mV, keeping V_s = V_{sub} = 0V [**1**]. The transistor is biased in the sub-threshold regime so that the channel is not fully conductive and the dopants in the channel have a larger interaction with the oxide defects. As seen in Fig. 1, the same set of signals show both correlated and uncorrelated fluctuations corresponding to two different defects that may be located at different distances from the Si-SiO_x interface.

Moreover, when some devices subject to SBD were studied at T = 77K and V_g = {0.5, 0.6}V and V_d = 100mV, two different correlation patterns of I_g - I_d were detected as seen in Fig. 2 [**1**]. In one case, both I_g and I_d decrease together and in the other, a lower I_d is accompanied by a higher I_g. With a multitude of these patterns observed, there are several explanations proposed. One postulation is that the defects in the amorphous IL layer could exhibit very different properties depending on the charge state of the vacancy (V_0^0, V_0^{1+}, V_0^{2+}). According to Liu *et al.* [**1**], neutral E' centers may become less effective in trap-assisted tunneling (TAT) conduction when electron capture occurs due to change in the thermal ionization and relaxation energy of the defects, while positive E' centers show exactly the opposite trend. In either case, the I_d is reduced because of the enhancement in the threshold voltage, V_{TH}. Another postulation is that the trapping / detrapping of electrons causes a local change in the oxide field which affects the TAT current [**2**].

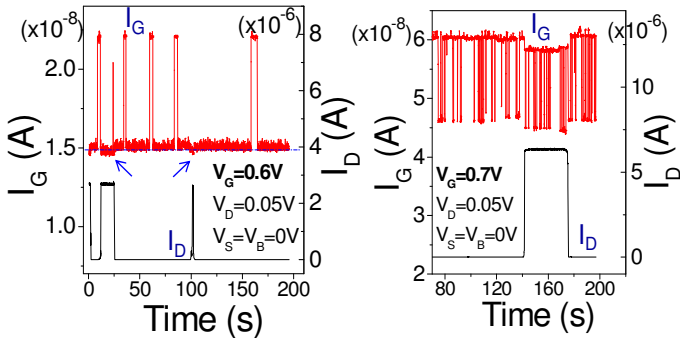

Figure 1. Observed I_g-I_d RTN trend at T = 150K showing one set of correlated signals and another set of uncorrelated signals embedded together, where these two signals correspond to two different defects in the dielectric (possibly located at very different locations from the Si-SiO_x interface) [**1**].

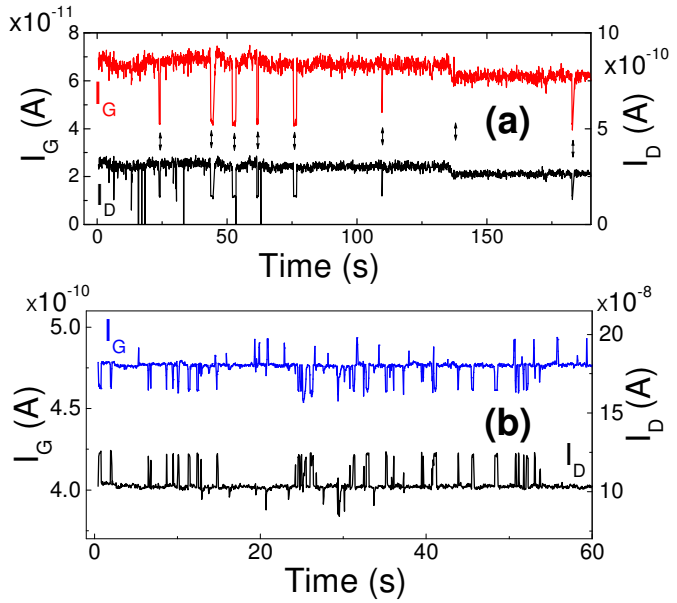

Figure 2. Observed I_g-I_d RTN trend at T = 77K showing (a) $I_g\downarrow$ ► $I_d\downarrow$ correlation measured at V_g/V_d = 0.5V/0.1V and (b) $I_g\downarrow$ ► $I_d\uparrow$ correlation measured at V_g/V_d = 0.6V/0.1V. Note that we are operating in the sub-threshold regime as V_{TH} was determined to be ~0.7V from post-SBD I_d-V_g measurements [**1**].

Using the phonon trap-assisted tunneling (PTAT) theory accounting for the inelastic effects [**4**, **5**] and making use of the voltage-dependent capture-emission time statistics, the location of the defects that correspond to the different I_g - I_d patterns was extracted (Fig. 3). As logically expected, defects deep inside the high-κ caused the uncorrelated signal (no RTN in I_d), while defects in the IL closer to the substrate showed the observed correlation in Figs. 1 and 2.

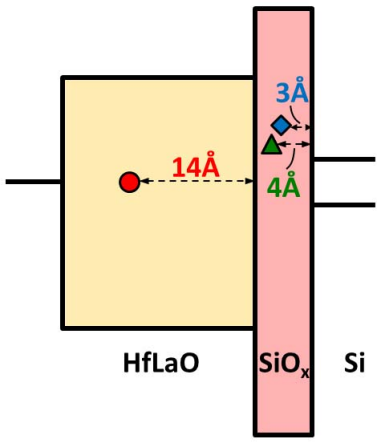

Figure 3. Band diagram showing the location of the three different defects responsible for the different I_g-I_d RTN patterns observed in Figs. 1 and 2 [**1**]. The defects situated deep in the high-κ layer was the one which showed uncorrelated I_g-I_d trends (the I_d was not perturbed at all due to the minimal interaction with the discrete dopants situated far in the channel).

The technology implications of these I_g - I_d patterns has not been dealt with adequately yet. The statistically random generation of defects in the dielectric stack results in a statistical correlation pattern between I_g and I_d signals. This in turn adds an additional stochastic variability component to the spread in V_{TH} and stress induced leakage currents (SILC) at the circuit level. Further work is needed to quantify these variations and better analytical models are needed to capture the percolation ideology being considered for channel conduction in transistors in the sub-threshold regime (with multiple potential barrier hills) [**6**, **7**].

III. Correlation of RTN and BTI

Several recent studies [**8**] – [**10**] have advocated that the RTN and BTI phenomena arise from the same common defects in the oxide. The relaxation phenomena in BTI with discrete steps of V_{TH} shift are shown to have the same time constant – voltage dependence trend as the RTN steady-state fluctuations though the two phenomena are sensed at different gate voltages and time scales. The current understanding is that some of the quick BTI relaxation events triggered at higher voltages may be observable as RTN only during prolonged device operation for several months / years and such defects with long capture / emission times can potentially result in the failure of critical circuits such as SRAM. A very recent investigation by Kerber [**11**] however refutes this understanding using a new diagnostic RTN measurement procedure. The author claims that while RTN and BTI may share some common traits, their time dependent evolution is very different. In fact, the author presents results that suggest that even after BTI stress, the RTN is unaffected, which means that the two phenomena do not go

hand in hand. It is suggested in Ref. [**11**] that post-BTI stress RTN characterization is not required at all and that any RTN impact on BTI is relevant only at time zero causing additional skew in the ΔV_{TH} distribution, while the impact of RTN at degradation levels close to the BTI failure criterion is negligible. With these contrasting opinions, there is no unified understanding on the BTI-RTN dependence and further in-depth characterization is still required in this context.

IV. Random Telegraph Noise in RRAM

Resistive RAM devices are particularly prone to RTN effects quite a lot due to their small size (scalability demonstrated down to 10 × 10 nm^2 [**12**]) and discrete defects located at a narrow constriction of the conductive filament [**13**] or located close to the vicinity of the filament impacting the conduction through Coulomb Blockade effects [**14**], more so in the high resistance state (HRS). There are two distinctive RTN trends observed in RRAM devices, one with steady state fluctuations at discrete levels (the standard RTN signature) and the other corresponding to non-steady state abrupt permanent jumps in the conduction level to high or low levels (known as "*disturb*").

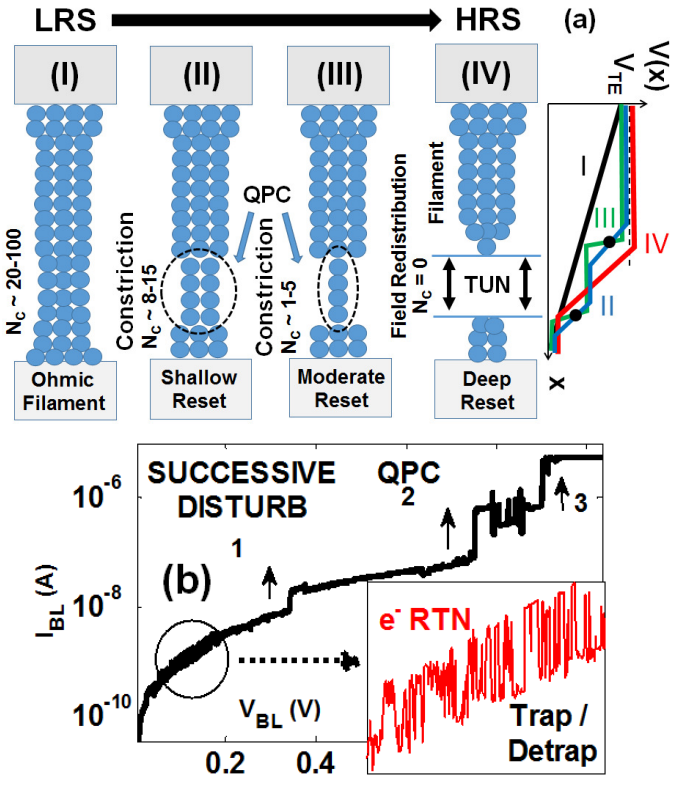

Figure 4. (a) Different possible configurations of the oxygen vacancy filament in RRAM from the LRS Ohmic state to intermediate higher states of resistance in the QPC mode to the deep reset state (HRS), referred to as the TUN mode [**15**]. The corresponding potential space profiles (V_{TE} refers to the voltage applied to the top electrode) for the four scenarios are shown in the right. In the case of QPC (moderate reset without filament rupture), there is high local field drop at two filament-constriction interfaces and it is this local field that exacerbates the read disturb issue. N_C refers to the number of oxygen vacancy defects in the constriction. (b) Observed multiple disturb trends in an RRAM device (at slow ramp rate of 10mV/sec) which cause permanent shift in conduction [**15**]. In this device, the first disturb event occurs at ~0.35V. The inset of the plot shows the standard electron capture-emission induced steady-state RTN where the filament configuration is not perturbed.

The standard voltages for SET and RESET in RRAM devices range between 0.5V and 1.5V (apart from initial forming which may require 2-4V). When the stored data is accessed ("read operation") typically at low read voltages of V_{READ} = 100mV, the disturb phenomena can be quite severe in the HRS state [**16**]. This is because although the voltage applied is low, the field distribution in the ruptured conductive filament in HRS can be highly localized and non-uniform as illustrated by Fig. 4(a) [**16**]. This localized field enhancement occurs in both possible configurations of the filament – tunnel barrier mode (TUN) and the quantum point contact (QPC) conduction mode [**15**]. As a result, the probability of vacancy perturbations in the filament and unintended change of memory state or shrinkage of memory window can be quite high. Studies on RTN disturb issues have remained quite phenomenological to date as it is hard to find straightforward analytical formulations that can accurately quantify the local field distributions for the TUN and QPC mode configurations of the filament [**17**]. Fig. 4(c) shows a typical multiple disturb trend in an RRAM device, where the first disturb event occurs at a relatively low voltage of 0.35V.

Even the steady-state RTN signals have a notable influence on the resistance variability and memory window in the RRAM device. When the RTN effects are superposed with the cycle-to-cycle intrinsic variability, the resulting variations can be quite detrimental, as recently highlighted by the work of Puglisi *et al.* [**18**, **19**]. The variation in the current ($\Delta I/I$) can be as high as 10-50% and this is more severe at low compliances, which is an issue when we push for ultra-low power switching devices. There is always a trade-off involved in the noise induced variation of resistive switching parameters and the power at which we intend to operate the device.

Many research groups are currently working towards making the RRAM device more immune to disturb events by tuning the material stack (altering the dielectric material) and the operating conditions. While endurance and retention failures have received sufficient attention, optimizing the RRAM for disturb immunity is still a key bottleneck to be resolved, given the difficulty in accurately modeling the phenomenon.

V. Probing Noise at the Nanoscale

While all the analysis in the previous sections talk about measuring and analyzing noise at the device level, a recent fascinating experiment to detect RTN on a blanket high-κ film was performed by Thamankar *et al.* [**20**]. In his work, the scanning tunneling microscope (STM) (with control current set at 50 pA so as to control the position and height of the Pt-Ir tip above the blanket film) was used to locally stress and then sense the noise arising from a very small number of defects. The dimension of stress coverage on the blanket film (5 nm thick HfO_2) ranged between 20-70 nm (depending on the quality of the tip and its curvature) and as shown by the preliminary results in Fig. 5, very clear RTN signals are detected. The use of STM for RTN studies can be an effective tool to better understand the differences (if any) in the properties of traps located at the grains, grain boundaries and triple points of polycrystalline dielectric films (which cannot be done at the device level). If the tip drift is well controlled and kept low, the results obtained can be quite reliable.

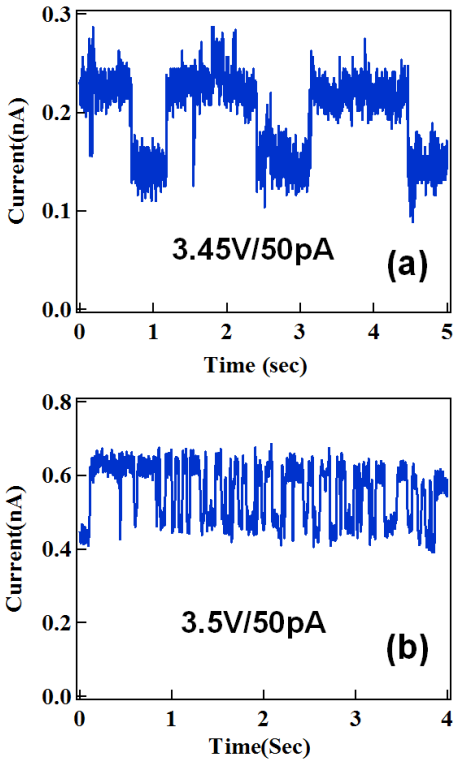

Figure 5. Observed RTN trends measured using an STM tip (with control current set at 50 pA) on a 5 nm HfO_2 dielectric film at two different tip voltages of (a) 3.45V and (b) 3.50V [**20**]. Note that only a fraction of this voltage drops across the dielectric when we account for the finite voltage drop across the vacuum gap between the tip and film.

To the best of our knowledge, this is one of the first efforts aimed at measuring RTN using the STM tool on blanket dielectric thin films. Further analysis is currently under way to explore the possibility of single defect probing using STM and in-depth spectroscopic analysis of these defects. The RTN study using STM will provide new ideas for tailoring the microstructure of high-κ dielectrics so that the desired noise immunity can be achieved through smart material and process design.

VI. Conclusion and Recommendation

A general review of the various RTN related issues in logic and memory devices has been presented in this study. Although RTN has been a mature field of study in microelectronics, there are many unsolved issues that deserve focus in the next few years. This includes the fundamental understanding behind why I_g and I_d show the different patterns of correlation and what this implies about the relative susceptibility of the HfO_2 and SiO_x to breakdown. The impact of I_g and I_d correlation on device level V_{TH} variability should be better modeled using analytical statistical models.

The new controversy on whether BTI and RTN are originating from the same type of defects has now come up and extensive electrical and atomistic studies would be needed to confirm the inter-relation between these two mechanisms. Are the two mechanisms caused by the same type of defects situated at different regions of the transistor or are they due to fundamentally different chemistry of the defects?

With RRAM beginning to replace Flash memory for future non-volatile memory applications, the need to better model read disturb issues and enhance the immunity of the memory device to these disturb problems is a key requirement. Associated to this is the need for more physical models to quantify the local field enhancements in the filament for the HRS state, be it the TUN mode or the QPC mode.

Lastly, as the potential for STM based RTN analysis is beginning to be harnessed, there are a lot of new opportunities available to characterize individual process and stress induced traps in detail, given the high spatial resolution and time resolution of measurements collected. With the evolution of new algorithms for decoding individual RTN components from multi-level RTN analysis [**21**, **22**], the STM based RTN studies can be a great new spectroscopy tool to study defects in novel high-κ materials once the dielectric film is deposited as a blanket film, even before the device is patterned on these substrates. We hope this short overview serves as a motivation and roadmap to follow for future high-κ noise analysis studies.

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